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Highly efficient and reliable high power InGaN/GaN LEDs with 3D patterned step-like ITO and wavy sidewalls

Jiajiang Lv[1,2], Chenju Zheng[1], Shengjun Zhou[*,1,3], Fang Fang[4], and Shu Yuan[5]

[1] School of Power and Mechanical Engineering, Wuhan University, Wuhan 430072, P.R. China
[2] Jiujiang Vocational and Technical College, Jiujiang 332007, P.R. China
[3] State Key Laboratory of Mechanical System and Vibration, School of Mechanical Engineering, Shanghai Jiao Tong University, Shanghai 200240, P.R. China
[4] Gold Medal Analytical and Testing Group, Guangzhou 510000, P.R. China
[5] Quantum Wafer, Inc., Foshan 528251, P.R. China

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[*] Corresponding author: e-mail zhousj@whu.edu.cn, Phone: +86 158 2734 8861, Fax: +86 027 6877 4381

Nitride-based high power LEDs with finger-like SiO_2 current blocking layer (CBL), three-dimensional (3D) patterned step-like ITO double layers and wavy sidewalls were fabricated. The finger-like SiO_2 CBL beneath finger-like p-electrode was designed to prevent current crowding effect, thereby facilitating uniform current spreading over the entire chip. In addition, 3D patterned step-like ITO double layers, including alternating 230 nm thick patterned upper step ITO layer and 100 nm thick lower step ITO layer, were formed by combining photolithography and aqua regia etchant. We showed that the top light extraction efficiency of high power LEDs can be significantly enhanced by taking 3D patterned step-like ITO. The light output power of high power LEDs with 3D patterned step-like ITO double layers is 13.9% higher than that of LEDs with smooth ITO layer. High-power LEDs with wavy sidewalls was fabricated by an optimized mask design in conjunction with dry etching process based on Cl_2/BCl_3 to improve light extraction efficiency at the horizontal direction. We demonstrated that light output power of high power LEDs with wavy sidewalls can be improved by 11% as compared to LEDs with flat sidewalls.

1 Introduction Gallium nitride-based materials have received considerable attention for the development of blue/green/ultraviolet light-emitting diodes (LEDs) [1–3]. The white-light source based on InGaN/GaN blue LED chip with phosphor coating is currently revolutionizing lighting, with the potential of saving huge amounts of energy every year [4, 5]. However, LEDs suffer from problem with insufficient external quantum efficiency (EQE). Generally, the EQE of LEDs depends on both the internal quantum efficiency (IQE) and the light extraction efficiency (LEE). The as-grown p-GaN layer is highly resistive due to high activation energy of magnesium (Mg) acceptors and relatively low hole mobility, current spreading at lateral direction of the LED structure was impeded, leading to undesirable current crowding effect around electrode pads and resulting photon absorption nearby electrode pads, which degrade device performance of top-emitting LEDs [6, 7]. Previously, indium-tin oxide (ITO) current spreading layer and SiO_2 current blocking layer (CBL) have been introduced to improve current spreading [8, 9]. Generally, an insulating SiO_2 CBL inserted underneath the ITO was used to uniformly redirect the current path and reduce the current crowding effect. Yet conventional SiO_2 CBL presents only a localized current blocking ability and, therefore, is not suitable for high power LED chip [10]. Moreover, the total internal reflection occurring at the interface between the GaN ($n = 2.5$), the smooth ITO ($n = 2.08$), and the ambient air ($n = 1$) limits the light extraction efficiency. It was previously demonstrated that the light extraction efficiency of LEDs can be improved by intentionally roughening LED surface [11–16]. A similar concept has also been applied to LED chip sidewalls, and more photons might escape from LEDs with textured sidewalls as compared to LEDs with

flat sidewalls [17, 18]. However, no study has reported on the combination of these methods to improve device performance of high power LEDs. In addition, high power LED with three-dimensional (3D) patterned step-like ITO has not yet been reported.

In this study, we demonstrated the application of a combination of finger-like SiO_2 CBL, 3D patterned step-like ITO double layers and wavy sidewalls for improving current spreading and light extraction efficiency of high power LEDs.

2 Experimental GaN-based LEDs were epitaxially grown on the cone-shaped patterned sapphire substrate by metal-organic chemical vapor deposition (MOCVD) equipment. Trimethylgallium (TMGa), trimethylindium (TMIn), and ammonia (NH_3) were used as precursors. Silane (SiH_4) and biscyclopentadienylmagnesium (Cp_2Mg) were used as the n- and p-dopant sources, respectively. These LED samples consist of a 30 nm thick GaN nucleation layer, a 1.5 μm thick undoped GaN buffer layer, a 2.15 μm thick Si-doped n-GaN layer, a InGaN/GaN multiple quantum well (MQW), a 40 nm thick Mg-doped p-AlGaN electron blocking layer, a 27 nm thick p-AlGaN/GaN superlattices, and a 110 nm thick Mg-doped p-GaN layer. The InGaN/GaN MQW structure consists of 12 pairs of 3 nm thick $In_{0.16}Ga_{0.84}N$ well and 12 nm thick GaN barrier layers. After GaN epitaxial growth process was completed, the LED wafer was subsequently annealed at 750 °C in N_2 atmosphere to activate Mg in the p-GaN layer.

Inductively coupled plasma (ICP) etching based on BCl_3/Cl_2 gas chemistry was employed to etch GaN mesa structure by removing a portion of p-GaN layer and MQW active layer to expose n-GaN layer. During the mesa fabrication process, a positive tone photoresist (EPG516, Everlight Chemical) mask layer was spin-coated onto LED wafer. Next, the EPG516 photoresist was patterned to be a rectangle shape with wavy sidewalls via photolithography process. Finally, GaN epitaxial layer was etched and wavy sidewalls in the photoresist mask layer could be transfer into scribing line along with the etched GaN mesa structure. During the etching process, the GaN etch rate was 136 nm min^{-1}, and GaN etch selectivity over phtoresist was 1.12 while maintaining 350 W ICP power/375 RF power, 60 sccm BCl_3/40 sccm Cl_2, and 5 mTorr operating pressure.

After forming wavy GaN sidewalls, a 190 nm thick finger-like SiO_2 CBL was subsequently formed on the top of p-GaN layer by plasma enhanced chemical vapor deposition (PECVD) and successive photolithography process and buffer oxide etching. To obtain 3D patterned step-like ITO double layers, a 230 nm thick ITO transparent conductive layer was deposited on the top of the finger-like SiO_2 CBL by an electron beam evaporator. The flat ITO was then selectively etched by combining photolithography and aqua regia etchant at etching condition of 38 °C for 60 s, and the etch depth between the upper step and the lower step was determined to be 130 nm. The circular pattern arrays were subsequently transferred into the upper step ITO layer by a combination of photolithography and aqua regia etchant again at etching condition of 38 °C for 30 s, and the etch depth was about 65 nm. A finger-like Cr/Pt/Au (20 nm/50 nm/1.5 μm) was deposited on the top of patterned step-like ITO and the exposed n-GaN layer as p- and n-electrode, respectively. The LED wafers were thinned down to be about 150 μm thick by mechanical grinding and polishing. Finally, the LED wafers were diced into chips with size of 1×1 mm^2.

We fabricated and characterized four types of high power LEDs with different device structures. LED I and II were fabricated to understand the usefulness of a finger-like SiO_2 CBL. LED III and IV were fabricated to investigate the usefulness of 3D patterned step-like ITO and wavy sidewalls. The schematic illustrations of LED I, II, III, and IV were shown in Fig. 1.

The properties of the fabricated LEDs were analyzed by optical microscopy, atomic force microscopy (AFM), and scanning electron microscopy (SEM). Current–voltage (*I–V*) characteristics of LEDs were measured using a semiconductor parameter analyzer (Keysight B2901A). The IQE, LEE, and EQE of each sample were determined by the Shockley–Read–Hall model method [19–21].

3 Results and discussion Figure 2a shows the etched mesa structure and the surrounding scribing line. The mesa etching depth is about 1.2 μm. During the mesa etching process, the scribing line for laser dicing was also defined at the same time. Figure 2b shows the optical microscopy image of finger-like SiO_2 CBL. Figure 2c shows the top-view SEM image of high power LED chip. As shown in Fig. 2c, the finger-like p-electrode aligned with SiO_2 CBL beneath the ITO was directly deposited on the top

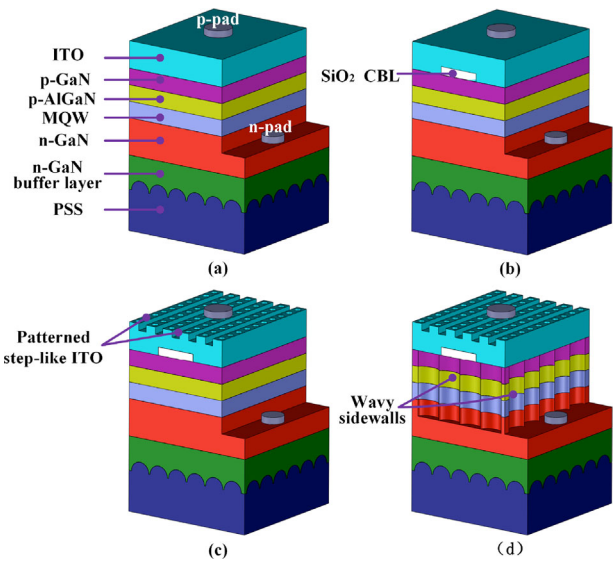

Figure 1 Schematic illustration of high power LEDs. (a) LED prepared on PSS (LED I). (b) LED prepared on PSS with SiO_2 CBL (LED II). (c) LED prepared on PSS with SiO_2 CBL and patterned step-like ITO (LED III). (d) LED prepared on PSS with SiO_2 CBL, 3D patterned step-like ITO, and wavy sidewalls (LED IV).

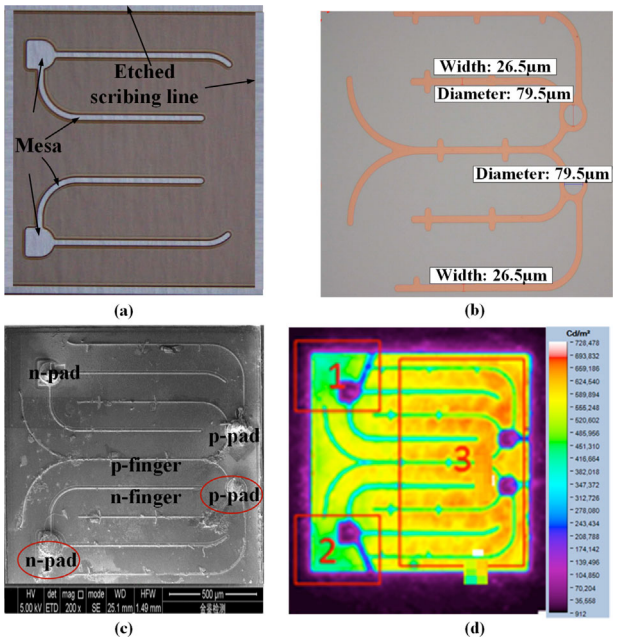

Figure 2 Demonstration of LED II with finger-like SiO_2 CBL and finger-like p-electrode. (a) Optical microscopy image of the etched mesa and scribing line. (b) Optical microscopy image of finger-like SiO_2 CBL. (c) Top-view SEM image of high power LED chip with finger-like p- and n-electrode. Scale bar, 500 μm. (d) Measured spatial distribution of light emission image.

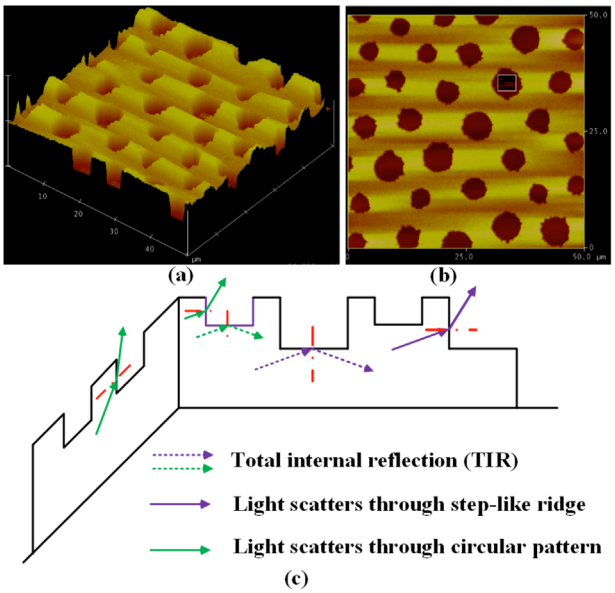

Figure 3 (a) AFM scanning image of LED III with 3D patterned step-like ITO double layers. The scanning area is $50 \times 50\ \mu m^2$. (b) Top-view AFM image of patterned step-like ITO double layers. The diameter of circular pattern is varied along the strip of upper step ITO layer ranging from 3.8 to 4.5 μm. (c) Schematic illustration of light propagation at the interface between the 3D patterned step-like ITO and the surrounding air.

of ITO, and the finger-like n-electrode was deposited on the top of etched mesa structure. The width of p-electrode is much less than that of SiO_2 CBL in order to prevent current concentration on regions immediately adjacent to the p-electrode. The width of n-electrode is also much less than that of mesa structure in order to prevent potential short circuit. Figure 2d shows the spatial distribution of light emission image for high power LEDs driven by injection current of 350 mA. As a higher density of current caused a stronger light emission, the spatial distribution of light emission image can be related to the distribution of injection current density. The current crowding effect occurring in high power LED with finger-like SiO_2 CBL, as shown in Fig. 2d, was almost negligible and the uniform current spreading over the entire chip was achieved due to the finger-like insulating SiO_2 CBL sandwiched between the ITO and the p-GaN, impeding the vertical current path, and thus enhancing the lateral current spreading performance.

Figure 3a shows AFM scanning image of 3D patterned step-like ITO double layers. The 3D step-like ITO double layers consisted of alternating 230 nm thick patterned upper step and 100 nm thick lower step, and circular pattern arrays orthogonal to the steps array were formed on the upper step ITO layer. The sidewall surface area extended in the vertical direction was able to be achieved by using 3D patterned step-like ITO, which can also contribute to improving light extraction efficiency owing to their 3D arrangement. Figure 3b shows top-view AFM image of patterned step-like ITO. The diameter of circular pattern ranges from 3.8 to 4.5 μm as shown in Fig. 3b. Figure 3c shows schematic illustration of light propagation at the interface between the 3D step-like ITO and the surrounding air. As shown in Fig. 3c, light emanated from MQW active region could experience multiple opportunities to find the escape cone by using the 3D patterned step-like ITO, leading to improvement in top light extraction efficiency of high power LED chip.

The SEM image of etched mesa structure was shown in Fig. 4a. The SEM image of wavy sidewalls was shown in Fig. 4b. The wavy sidewalls can ensure that the photons emanated from MQW active region have a larger probability to be escaped from high power LEDs via textured GaN

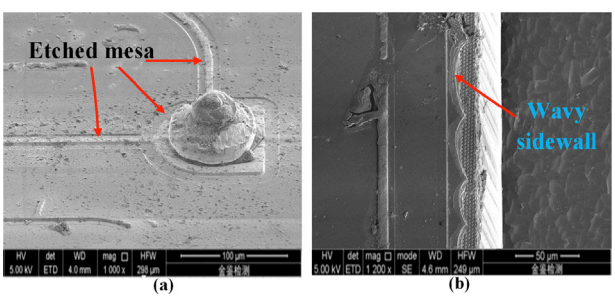

Figure 4 (a) SEM image of etched mesa structure and the deposited n-electrode. Scale bar, 100 μm. (b) SEM image of wavy sidewalls. Scale bar, 50 μm.

sidewalls, thereby enhancing light extraction efficiency at the horizontal direction [18].

High power blue LED chips with size of $1 \times 1\,mm^2$ were wire bonded onto lead frame and then were encapsulated by silicone resin. The peak wavelength of high power LEDs measured at 350 mA was around 456 nm. The light output powers of LEDs were measured using an integrating sphere. The light output powers of LEDs versus injection current were shown in Fig. 5. With injection current of 350 mA, the light output powers of LED I, II, III, and IV were 430, 486, 554, and 615 mW, respectively. The light output power of LED II was 13% higher than that of LED I, which was attributed to improved current spreading performance and thus more uniform carrier distribution over the entire chip via finger-like p-electrode and underlying finger-like SiO_2 CBL. The light output power of LED III was about 13.9% higher than that of LED II, which was ascribed to an enhancement in top light extraction efficiency by using 3D patterned step-like ITO. The light output power of LED IV with wavy sidewalls was 11% higher than that of LED III. This enhancement was attributed to the wavy sidewalls, which increased scattering probability of photons at the interface between the GaN sidewalls and the surrounding air and thus improved light extraction efficiency at the horizontal direction.

Figure 6 shows the *I*–*V* curves of high power LEDs. With injection current of 350 mA, the forward voltages (V_f) of LED I, II, III, and IV were 3.077, 3.102, 3.131, and 3.137 V, respectively. As the finger-like SiO_2 CBL was sandwiched between the ITO and the p-GaN layer, the total ohmic contact area between the ITO layer and the p-GaN layer would decline due to the insulating characteristic of SiO_2 CBL, thereby leading to an increase in series resistance. Owing to increased series resistance along the vertical current path, the forward voltage of LED II was greater than that of LED I. It was found that forward voltage of LED III with 3D patterned step-like ITO was higher than

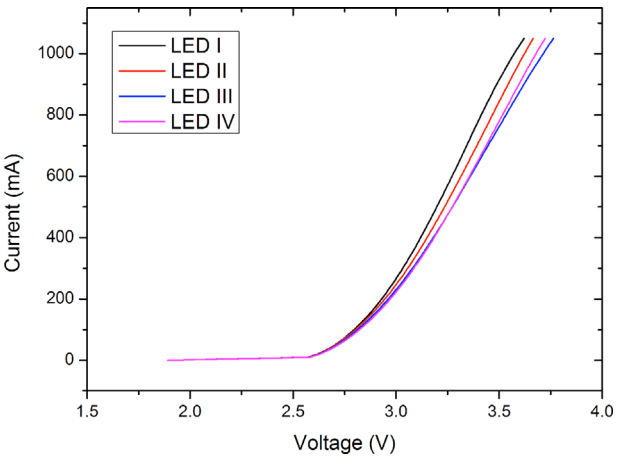

Figure 6 Current–voltage characteristics of high power LEDs.

that of LED II. The slightly higher forward voltage originated from the patterned step-like ITO that impeded lateral current spreading. The 350 mA driven forward voltages were both around 3.13 V for the LED IV with wavy sidewalls and the LED III with flat sidewalls. Accordingly, the wavy sidewalls would not cause any degradation in the electrical properties of high power LEDs.

The reverse leakage current (I_R), which is well correlated with device reliability, lifetime, and degradation under high power operating condition, should be as low as possible [22, 23]. The distribution of I_R value for high power LEDs was measured at negative bias (at −7 V) using a wafer-level probe station system. The total number of LED chips with size of $1 \times 1\,mm^2$ from a 2 in. wafer was about 1265. Figure 7 shows the distribution of I_R value for the four fabricated high power LEDs in wafers. More than 90% of LED I, II, III, and LED IV have I_R value less than 0.75 μA. The distribution of I_R value less than 0.25 μA for LED I, II, III, and LED IV was 36.35%, 37.06%, 35.62%, and 33.75%,

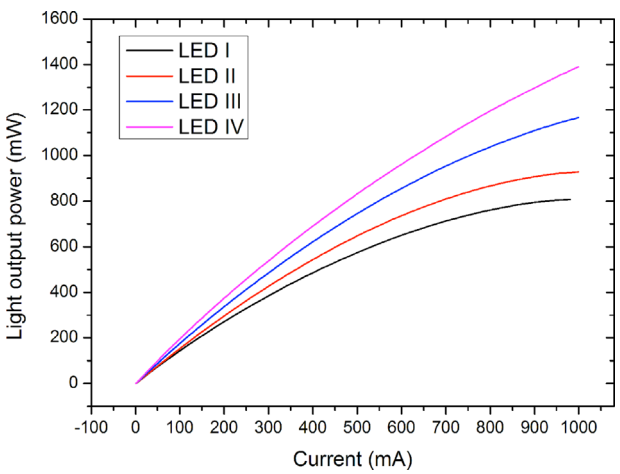

Figure 5 Light output power of high power LEDs with different device structures versus injection current.

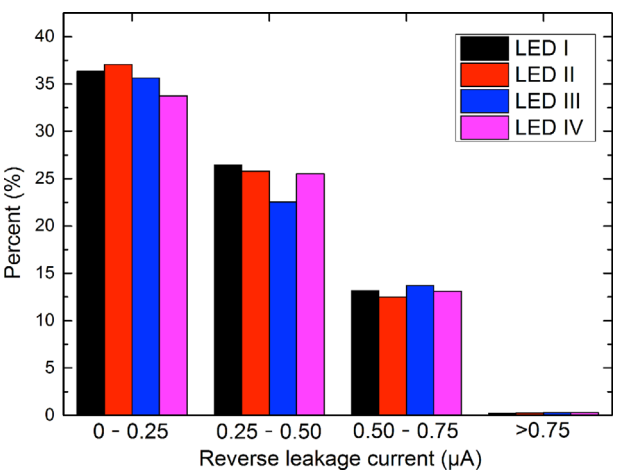

Figure 7 Distribution of reverse leakage current of high power LEDs in wafers.

Table 1 IQE, LEE, EQE, and wall-plug efficiency (WPE) of high power LEDs at 350 mA.

	IQE [%]	LEE [%]	EQE [%]	WPE [%]
LED I	79	57.2	45.2	39.9
LED II	79	64.7	51.1	44.8
LED III	79	73.7	58.2	50.6
LED IV	79	81.8	64.6	56.0

respectively. The distribution of I_R value located between 0.25 and 0.5 μA for LED I, II, III, and LED IV was 26.43%, 25.80%, 22.55%, and 26.43%, respectively. In other words, the distribution of I_R value for LED I, II, III, and IV was nearly the same or similar, which indicated that the 3D patterned step-like ITO and wavy sidewalls did not induce excess current leakage path.

Table 1 summarized the IQE, LEE, and EQE of each sample. The EQE and LEE of the LED IV were, respectively, 64.6% and 81.8% at an injection current of 350 mA.

For white LEDs packaging, the high power blue LED chips were attached on lead frame with adhesive, the gold wire bonding process was subsequently conducted to provide electrical interconnection, and a 70 μm thick phosphor layer was directly coated on the blue LED chip. We measured the luminous flux of packaged high power white LEDs by using integrating sphere. Figure 8 shows the comparison of luminous flux of fabricated high power LED IV and commercial LEDs. The luminous efficiency of mass-produced high power LED IV with a size of $1 \times 1\,mm^2$ was greater than $150\,lm\,W^{-1}$ when combining finger-like SiO_2 CBL, 3D patterned step-like ITO, and wavy sidewalls. Moreover, the degradation of packaged LEDs, as shown in Fig. 8, was also investigated at the condition of 85 °C and 85% relative humidity using an injection current of 350 mA. The optical degradation of fabricated high power LED IV was lower than that of commercial LEDs after 168 h accelerated lifetime tests.

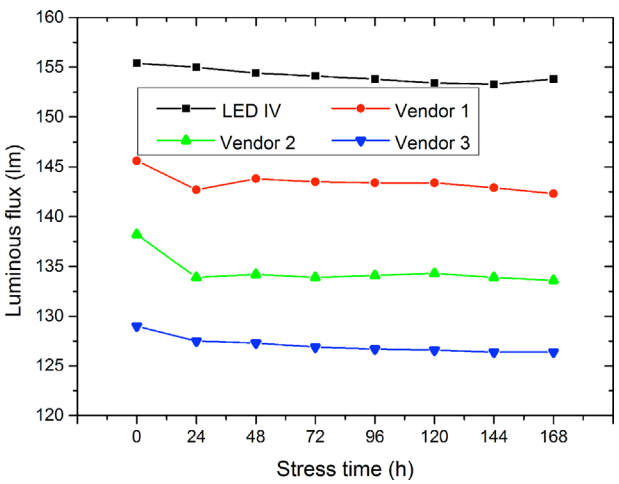

Figure 8 Comparison of luminous flux of fabricated high power LED IV and commercial LEDs.

4 Conclusions High power LEDs with finger-like SiO_2 CBL, 3D patterned step-like ITO double layers, and wavy sidewalls were fabricated. The light output power of LED II with finger-like SiO_2 CBL was 13% higher than that of LED I without finger-like SiO_2 CBL owing to improved current spreading performance. The light output power of LED III with 3D patterned step-like ITO was about 13.9% higher than that of LED II, which was ascribed to an enhancement in top light extraction efficiency by using 3D patterned step-like ITO. The light output power of LED IV with wavy sidewalls was 11% higher than that of LED III due to improved light extraction efficiency at the horizontal direction. The luminous efficiency of mass-produced high power LEDs with a size of $1 \times 1\,mm^2$ were greater than $150\,lm\,W^{-1}$ (at 350 mA) when combining finger-like SiO_2 CBL, 3D patterned step-like ITO and wavy sidewalls.

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References

[1] C. Weisbuch, M. Piccardo, L. Martinelli, J. Iveland, J. Peretti, and J. S. Speck, Phys. Status Solidi A **212**, 899 (2015).
[2] H. Riechert, Phys. Status Solidi A **212**, 893 (2015).
[3] K. C. Shen, W. Y. Lin, H. Y. Lin, K. Y. Chen, and D. S. Wuu, Opt. Express **22**, 17600 (2014).
[4] T. X. Yan, J. He, W. Yang, K. Rajabi, W. H. Chen, J. J. Wu, X. N. Kang, G. Y. Zhang, and X. D. Hu, Phys. Status Solidi A **212**, 925 (2015).
[5] S. Zhou, B. Cao, S. Yuan, and S. Liu, Appl. Opt. **53**, 8104 (2014).
[6] J. Herrnsdorf, E. Xie, I. M. Watson, N. Lauran, and M. D. Dawson, J. Appl. Phys. **115**, 084503 (2014).
[7] Y. J. Liu, C. C. Huang, T. Y. Chen, C. S. Hsu, J. K. Liou, and W. C. Liu, IEEE J. Quantum Electron. **47**, 755 (2011).
[8] S. Zhou, S. Yuan, Y. Liu, L. Jay, Guo, S. Liu, and H. Ding, Appl. Surf. Sci. **355**, 1013 (2015).
[9] J. K. Liou, C. C. Chen, P. C. Chou, S. Y. Cheng, J. H. Tsai, R. C. Liu, and W. C. Liu, IEEE Trans. Electron Devices **60**, 2282 (2013).
[10] J. K. Liou, C. C. Chen, P. C. Chou, T. Y. Tsai, S. Y. Cheng, and W. C. Liu, Solid-State Electron. **99**, 21 (2014).
[11] S. Zhou, S. Liu, and H. Ding, Opt. Laser Technol. **47**, 127 (2013).
[12] J. Z. Liu, M. D. B. Charlton, C. H. Lin, K. Y. Lee, C. Krishnan, and M. C. Wu, IEEE J. Quantum Electron. **50**, 314 (2014).
[13] M. Ohya, K. Naniwae, T. Kondo, A. Suzuki, M. Mori, T. Kitano, A. Usui, and S. Kamiyama, Phys. Status Solidi A **212**, 935 (2015).
[14] K. Huang, Y. C. Gan, Q. K. Wang, and X. S. Jiang, Opt. Laser Technol. **72**, 134 (2015).
[15] Y. Zhang, J. Li, T. Wei, J. Liu, X. Yi, G. Wang, and F. Yi, Jpn. J. Appl. Phys. **51**, 020204 (2012).

[16] T. Fujii, Y. Gao, R. Sharma, E. L. Lu, S. P. DenBaars, and S. Nakamura, Appl. Phys. Lett. **84**, 855 (2004).
[17] Y. Y. Zhang, E. Q. Guo, Z. Li, T. B. Wei, J. Li, X. Y. Yi, and G. H. Wang, IEEE Photon. Technol. Lett. **24**, 243 (2012).
[18] C. S. Chang, S. J. Chang, Y. K. Su, C. T. Lee, Y. C. Lin, W. C. Lai, S. C. Shei, J. C. Ke, and H. M. Lo, IEEE Photon. Technol. Lett. **16**, 750 (2004).
[19] Q. Dai, M. F. Schubert, M. H. Kim, J. K. Kim, E. F. Schubert, D. D. Koleske, M. H. Crawford, S. R. Lee, A. J. Fischer, G. Thaler, and M. A. Banas, Appl. Phys. Lett. **94**, 111109 (2009).
[20] K. Takeda, F. Mori, Y. Ogiso, T. Ichikawa, K. Nonaka, M. Iwaya, S. Kamiyama, H. Amano, and I. Akasaki, Phys. Status Solidi C **7**, 1916 (2010).
[21] C. L. Xu, T. J. Yu, J. Yan, Z. Y. Yang, X. B. Li, Y. B. Tao, X. X. Fu, Z. Z. Chen, and G. Y. Zhang, Phys. Status Solidi C **9**, 757 (2012).
[22] Q. F. Shan, D. S. Meyaard, Q. Dai, J. Cho, E. Fred, Schubert, J. K. Son, and C. Sone, Appl. Phys. Lett. **99**, 253506 (2011).
[23] X. A. Cao, P. M. Sandvik, S. F. LeBoeuf, and S. D. Arthur, Microelectron. Reliab. **43**, 1987 (2003).

