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Improved light output power of LEDs with embedded air voids structure and SiO_2 current blocking layer

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ABSTRACT

GaN-based light-emitting diodes (LEDs) with an embedded air voids structure and a SiO_2 current blocking layer (CBL) was fabricated and investigated. The air voids structure was formed between cone-shaped patterned sapphire substrate and GaN epitaxial layer by combining laser scribing with H_3PO_4-based hot chemical etching. The air voids embedded high power LED showed 8.9% higher light output power due to a strong light reflection and redirection at the interface between GaN and air voids, which could increase the top light extraction of the high power LED. Compared to the air voids embedded high power LED, the light output power of the high power LED by integrating air voids structure with SiO_2 CBL was 9.1% higher than that of the air voids embedded LED without SiO_2 CBL. It was also found that the simulation results agree well with the experimental results.

1. Introduction

Light-emitting diodes (LEDs) have advantages of long lifetime, low energy consumption, and compactness with respect to other electric light sources such as incandescent lamps. Due to its numerous advantages, LEDs have been widely used in full-color displays, traffic signals, backlights for cell phone and also has considerable potential in general lighting applications. However, LEDs suffer from problem with insufficient external quantum efficiency (EQE). Generally, the EQE of LEDs depends on both the internal quantum efficiency (IQE) and the light extraction efficiency (LEE). The IQE of LED is limited by high dislocation density, strong piezoelectric filed in quantum wells, and low hole concentration of *p*-GaN layer. The LEE is limited by the total internal reflection occurring along the GaN/air and sapphire/air interface because the refractive indexes of GaN and sapphire substrate are much higher that of air, which would result in a critical angle for the light escape cone according to Snell's law. The light outside the escape cone is therefore trapped in the LED epitaxial layer and can be reabsorbed by the active layers and metal electrodes, resulting in a decrease in light output power of LEDs.

Due to the total internal reflection, only approximately 4% of the internal light can be extracted from the surface of the conventional GaN-based LED to the air. Numerous methods have been applied for improving the LEE of the LED, such as textured surfaces [1], surface microstructure [2], photonic crystal [3], patterned indium tin oxide (ITO) [4], current blocking layer [5], graded-refractive-index antireflection coatings [6], patterned sapphire substrate (PSS) [7], and bottom reflectors [8]. In particular, it was well known that PSS technology can improve not only the LEE due to the angled facets that redirected light into the escape cone but also the IQE by the reduction of dislocation density. It is also possible to enhance LEE of LEDs by forming air voids at GaN/PSS interface by chemical etching [9,10]. The current crowding around the p-electrode pad can be effectively alleviated by using the current blocking layer, which can improve both electrical and optical performance of LED.

To achieve higher light output power, the electrical power and the size of LED chip must be increased. Accordingly, high power LED chip is a development goal for general lighting. However, most of the above-mentioned methods have been successfully applied to small size of LED chip with low input power, and few studies focused on the high power LED. In this paper, both air voids structure and current blocking layer was employed to improve the LEE of high power LED chip. In this design, an inverted cone shaped air voids structure was embedded between a patterned sapphire substrate and a GaN buffer layer by combining laser scribing with H_3PO_4-based hot chemical etching process to improve the top LEE of the high power LED, and a SiO_2 CBL inserted beneath the p-electrode pad was utilized to improve current spreading performance of the high power LED. Optical simulations of the air

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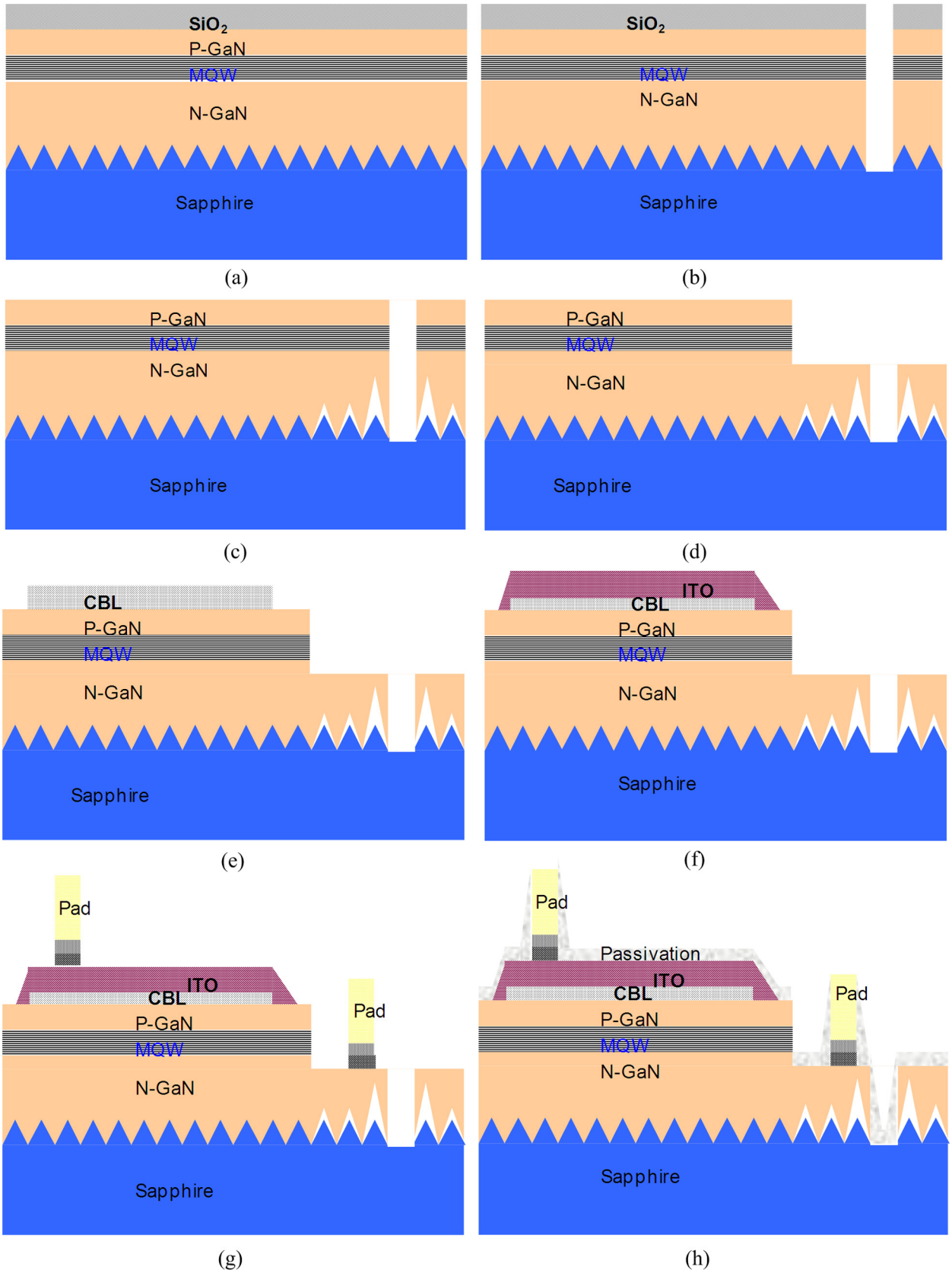

Fig. 1. Fabrication process of the high power LED with embedded air voids structure and SiO_2 CBL.

voids embedded LEDs were also performed and compared with the experimental results.

2. Experiments

LED epitaxial layer was grown on the PSS by metal organic chemical vapor deposition (MOCVD) system. Trimethylgallium (TMGa), trimethylindium (TMIn), and ammonia (NH_3) were used as precursors. Silane (SiH_4) and biscyclopentadienymagnesium (Cp_2Mg) were used as the n-dopant and p-dopant source. The LED epitaxial layer consists of a 30-nm-thick GaN nucleation layer, a 1.5-μm-thick undoped GaN buffer layer, a 3-μm-thick Si-doped *n*-GaN layer, a InGaN/GaN multiple quantum well (MQW), a 100-nm-thick Mg doped *p*-AlGaN electron blocking layer, and a 190-nm-thick Mg-doped *p*-GaN layer. The InGaN/GaN MQW structure consists of twelve pairs of 3-nm-thick $In_{0.16}Ga_{0.84}N$ well layers and 12-nm-thick GaN barrier layer. After the epitaxial growth process, the LED wafer was subsequently annealed at 750 °C in N_2 atmosphere to active Mg in the p-GaN layer.

The fabrication process flow diagrams of the high power LED by integrating air voids structure with SiO_2 CBL were shown in Fig. 1. The detailed proceeding steps were illustrated in the following: (a) a 3.0-μm-thick SiO_2 was deposited onto LED wafer to serve as the protection layer during wet etching process; (b) nanosecond laser scribing was then performed to scribe the LED wafer along the designed scribing line. The nanosecond pulse laser has a wavelength of 355 nm, a repetition rate of 50 kHz, and an average output power of 1 W. The depth and width of the laser-scribed trench are 15 μm and 5 μm, respectively; (c) the scribed samples were then wet etched by a mixture of H_3PO_4 and H_2SO_4 solution (H_3PO_4:H_2SO_4 = 3:1) at 260 °C for 6 min (LED II), or 15 min (LED III), or 20 min (LED IV), respectively, and the SiO_2 protection layer was removed by buffer oxide etch solution after the H_3PO_4-based hot chemical etching process; (d) $Cl_2/BCl_3/Ar$ inductively coupled plasmas was used to etch the LED samples until the *n*-GaN layer was exposed, and the etch depth was 1.2 μm; (e) A 182-nm-thick SiO_2 CBL was subsequently deposited on *p*-GaN surface by plasma enhanced chemical vapor deposition (PECVD), and a 19-μm-width CBL pattern was defined by using standard photolithography and wet etching process; (f) a 100-nm-thick indium tin oxide (ITO) layer was then deposited on the p-GaN layer as current spreading layer by using an electronic beam evaporator; (g) a Cr/Pt/Au multi-layer films were deposited onto the exposed n-GaN layer and the ITO layer to serve as the n-electrode and p-electrode, respectively; (h)

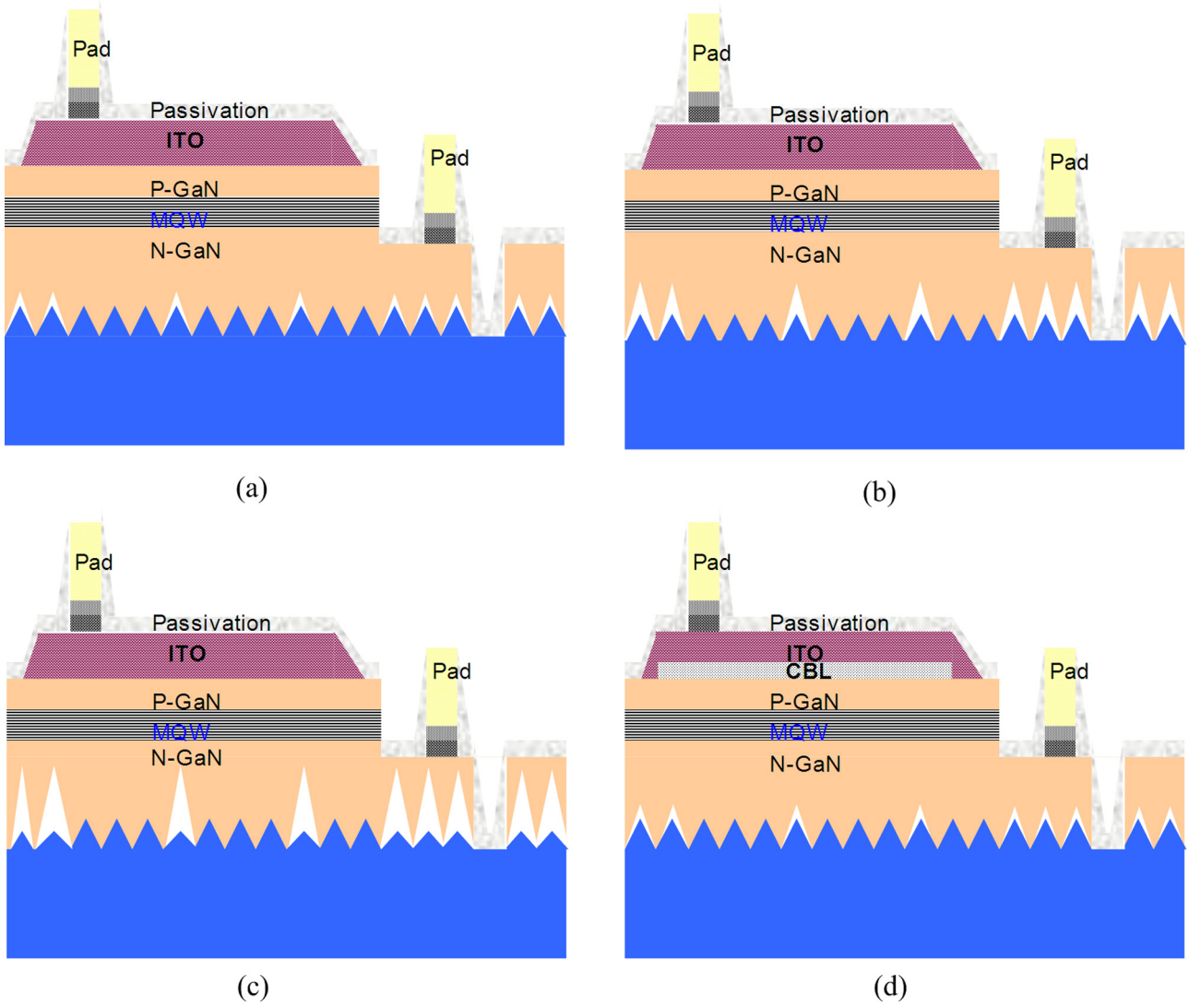

Fig. 2. Schematic diagrams of (a) LED II prepared on PSS with 6 min H_3PO_4-based hot chemical etching, (b) LED III prepared on PSS with 15 min H_3PO_4-based hot chemical etching, (c) LED IV prepared on PSS with 20 min H_3PO_4-based hot chemical etching, and (d) LED V prepared on PSS with 6 min H_3PO_4-based hot chemical etching and SiO_2 CBL.

A 69-nm-thick SiO_2 passivation layer was deposited on the LED surface by PECVD. Finally, LED wafers were thinned to about 150 μm by using backside lapping and polishing and broken into chips with size of 45 mil × 45 mil.

For comparison, the conventional LED grown on PSS (LED I) without air voids structure and CBL was prepared, and the LED V with air voids structure and SiO_2 CBL was also prepared. The schematic diagrams of the LED II, LED III, LED IV, and LED V were shown in Fig. 2. The LED II, LED III, and LED IV have different height of air void structure. The LED V and LED II have the same height of air void structure. Unlike the LED II, the LED V consists of not just air void structure, but rather of SiO_2 CBL. The scanning electron microscopy (SEM) and transmission electron microscopy (TEM) were used to evaluate cross-sectional profile of LED samples. Current–voltage (*I*–*V*) characteristics of LEDs were measured by a probe station system. Light output power of LEDs was measured by using an integrating sphere.

3. Results and discussion

The PSS was fabricated by combining a thermally reflowed photoresist technique and an inductively coupled plasma (ICP) etching method [11]. First, a negative photoresist (NR71-3000P, Futurrex) of 4-μm-thick was spin-coated on the *c*-plane (0 0 0 1) flat sapphire substrate. The photoresist was then patterned to be a circular shape by standard photolithography and reflowed during a hard baking process at 125 °C to make a cone-shaped pattern. Subsequently, the sapphire substrate was etched by employing BCl_3/Ar plasmas, and periodic cone-shaped patterns were formed on the sapphire substrate. During the ICP etching process, SEM images of sapphire at different etching time was shown in Fig. 3. Fig. 3(a) indicated that the sidewalls of patterns were almost vertical before the photoresist shrank. However, with the increasing etching time, the sidewalls, as shown in Fig. 3(b)–(d), were tapered as the photoresist shrank and the top surface of patterns was exposed to plasmas.

Fig. 4 showed the TEM image of LED epitaxial layer grown on the PSS with periodic cone shaped patterns (2.5 μm diameter, 1.5 μm height, and 0.5 μm spacing). As shown in Fig. 4, it was found that the entire substrate was covered by GaN epitaxial layer. This is due to the use of cone shaped PSS which can significantly enhance the lateral growth of GaN. It was also noted that the threading dislocation density in the vicinity of GaN/PSS interface was higher than that away from the interface.

The cross-sectional SEM images of the LED II, LED III, LED IV were shown in Fig. 5. The inverted cone shaped air-void structure, as shown in Fig. 5, was formed between the PSS and GaN epitaxial layer after laser scribing and H_3PO_4-based hot chemical etching. The etching rate of GaN in the vicinity of GaN/PSS interface should

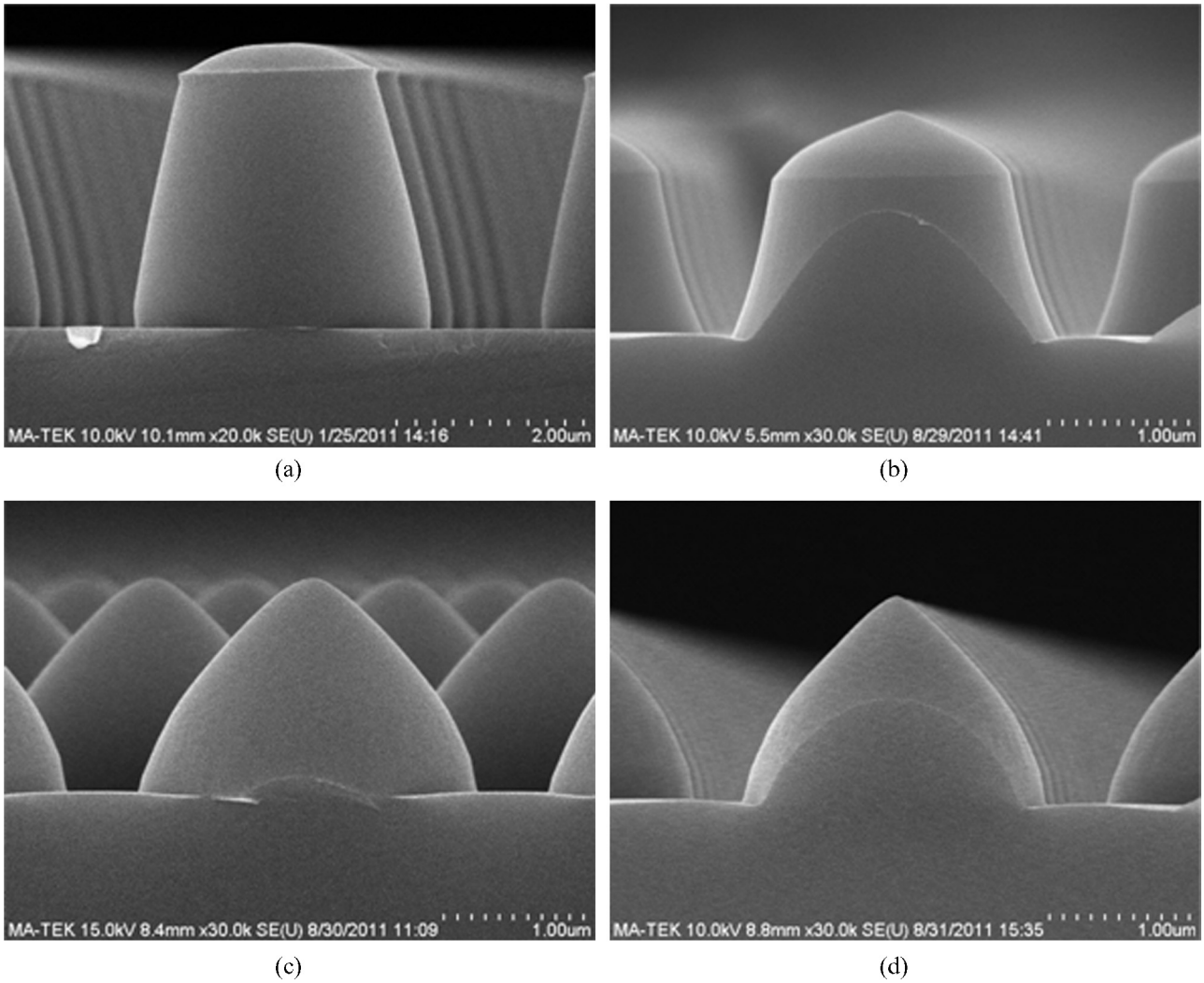

Fig. 3. SEM images of sapphire at different etching times: (a) 10 min, (b) 20 min, (c) 30 min, and (d) 35 min. Process condition: 1500 W/300 W of ICP/RF power, 7 mTorr of operating pressure, 50 sccm/10 sccm of BCl_3/Ar flow rate.

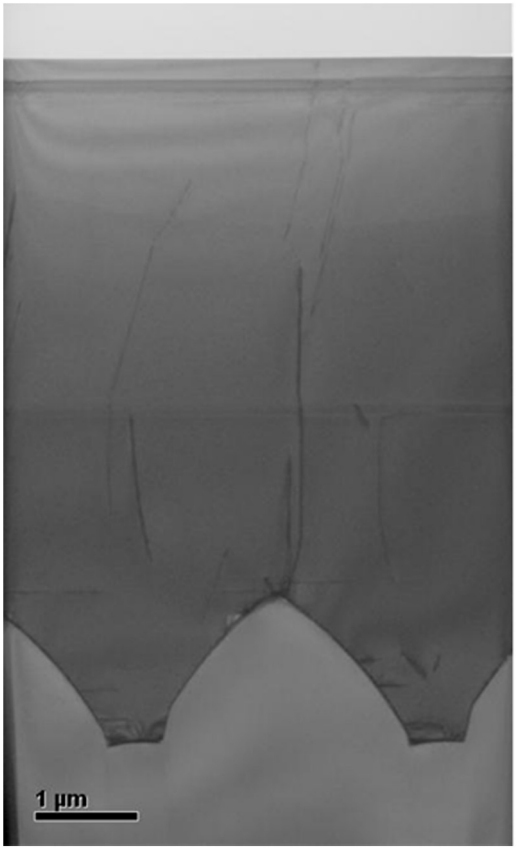

Fig. 4. TEM image of the LED epitaxial layer grown on the PSS.

be much higher than that away from the interface because the threading dislocation density in the vicinity of GaN/PSS interface, as shown in Fig. 4, was higher than that away from the interface, especially the vicinity of GaN/PSS peak interface. Through defect-selective etching, the air voids structure was formed between the cone-shaped PSS and GaN epitaxial layer. As the wet etching time was increased from 6 min to 20 min, the average height of the air voids structure was 3 μm (LED II), 4.5 μm (LED III), and 4.8 μm (LED IV), respectively. Meanwhile, the cone-shaped PSS was also etched, causing the reduction in the size of cone-shaped PSS, and the average height of cone-shaped PSS was 1.5 μm, 0.7 μm, and 0.5 μm, respectively.

Fig. 6 showed the SEM image of the LED V with SiO_2 CBL deposited beneath the *p*-electrode pad. A 182-nm-thick insulating SiO_2 CBL underneath the 100-nm-thick ITO transparent conductive layer, as shown in Fig. 6, was used to deflect the current away from the *p*-electrode, resulting in better current spreading performance. A 69-nm-thick SiO_2 passivation layer was deposited on the top of ITO transparent conductive layer, which can reduce the reverse leakage current and enhance the reliability of the high power LED chip.

Fig. 7 showed the light output power of the fabricated five LEDs as a function of injection current. The measured light output power of LEDs by using an integrating sphere corresponds to the radiant power of electromagnetic radiation of a light source, and the unit of radiant power is the Watt [W]. Therefore, we used the unit (milli-Watt, mW) for the dimension of the vertical axis in Fig. 7. At 350 mA injection current, the light output powers of the five LEDs were 436 mW, 475 mW, 471 mW, 465 mW, 518 mW for the LED I, LED II, LED III, LED IV, and LED V, respectively. The light output power of the LED II was 8.9% higher than that of the LED I, which was primarily attributed to the increased light extraction through the top

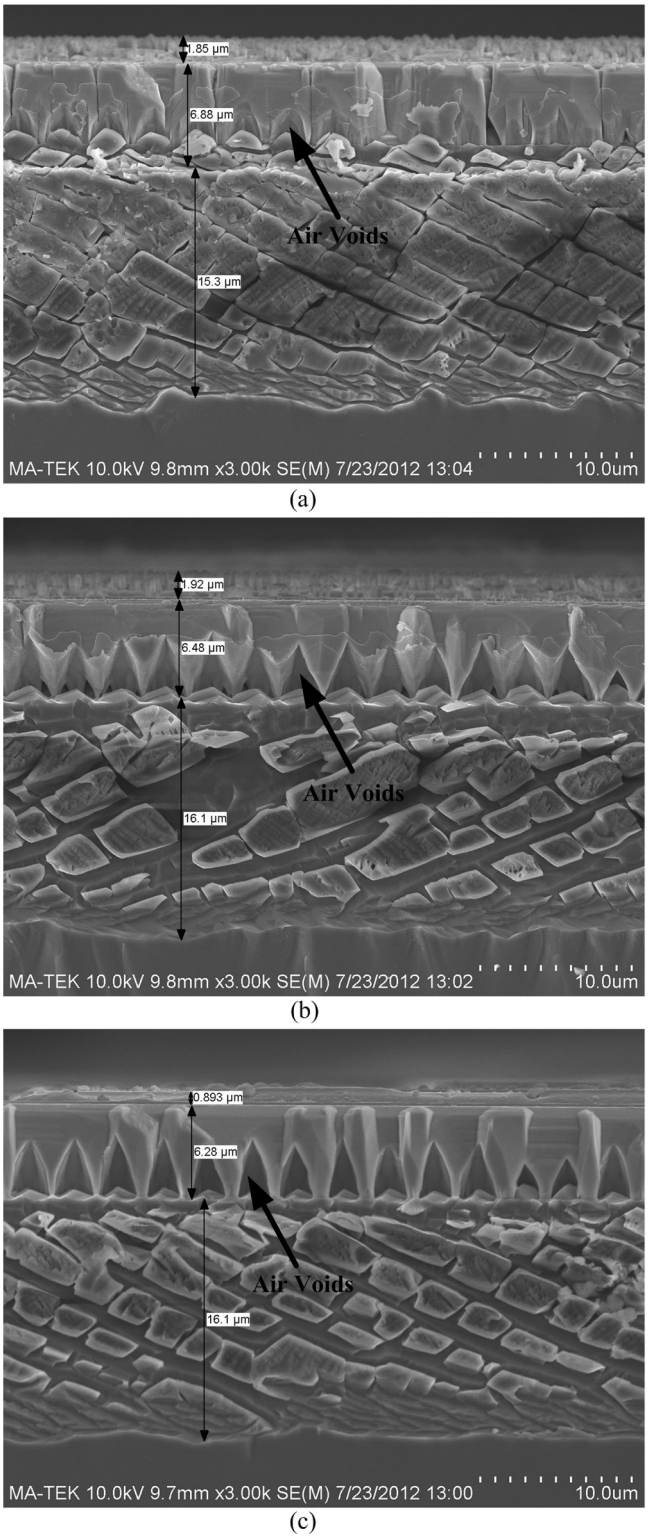

Fig. 5. Cross-sectional SEM images of (a) LED II, (b) LED III, and (c) LED IV.

face due to a strong light reflection and redirection by the air voids [9]. Moreover, the light output power of LED II was slightly larger than that of LED III and LED IV. The light output power of LED V was 9.1% higher than that of LED II under 350 mA injection current. This enhancement was attributed to the improved current spreading performance and the increased current injection into the MQW active layer of the high power LED chip by employing SiO_2 CBL. The light output saturation current of LED I, LED II, LED III, LED IV, and

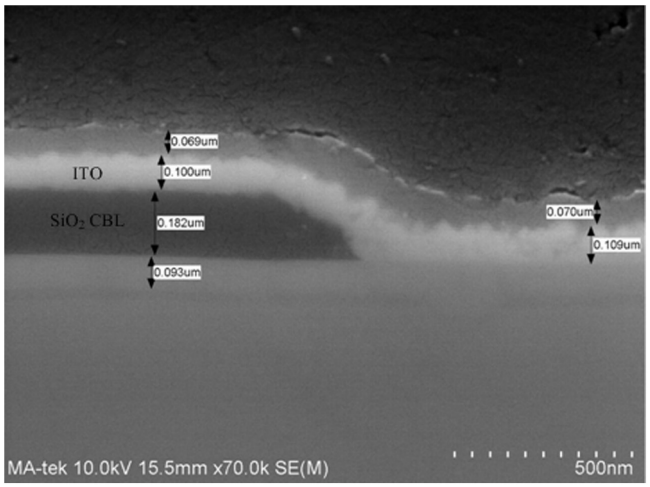

Fig. 6. SEM image of the LED V with SiO_2 CBL deposited beneath *p*-electrode pad.

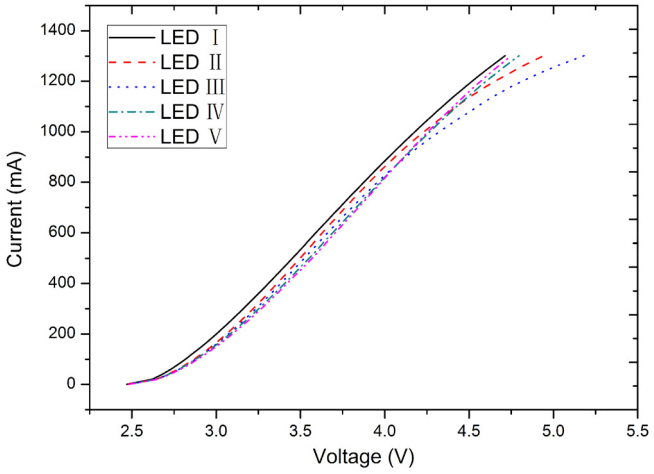

Fig. 8. *I–V* characteristics of LEDs with different structure.

LED V were 1021 mA, 1010 mA, 1021 mA, 1000 mA, and 1130 mA, respectively. The LED II and LED IV showed larger efficiency droop than other LEDs. The fluctuations of LED epitaxial structure may be the reason for the occurrence of this phenomenon. Additionally, the light output saturation current of LED V was significantly larger than other LEDs, which may be also attributed to the alleviated current crowding around *p*-electrode pad by the use of SiO_2 CBL, leading to the reduction in efficiency droop.

Fig. 8 showed the *I–V* (current–voltage) curves of the fabricated five LEDs. At 350 mA injection current, the forward voltages (V_f) of the fabricated five LEDs were 3.27 V, 3.32 V, 3.35 V, 3.36 V, and 3.39 V for LED I, LED II, LED III, LED IV, and LED V, respectively. The 350-mA-driven wall-plug efficiency of the fabricated five LEDs was 38.09%, 40.87%, 40.16%, 39.54%, 43.65% for the LED I, LED II, LED III, LED IV, and LED V, respectively, which was much higher than that of the reported LEDs with patterned sapphire and patterned ITO in the previous literature [4]. Compared to the conventional LED, a slightly increased V_f for the air voids embedded LEDs was observed, which could be attributed to the incomplete covering of the SiO_2 protection layer during the H_3PO_4-based hot chemical etching process, resulting in surface damage of p-GaN layer and thus higher serial resistances [12]. In contrast to the air voids embedded LED, a slightly increased V_f for the LED with SiO_2 CBL was also observed, which was attributed to the reduction in the total area of the p-type metal contact between the ITO layer and the p-GaN layer as a result of the presence of the insulating SiO_2 layer.

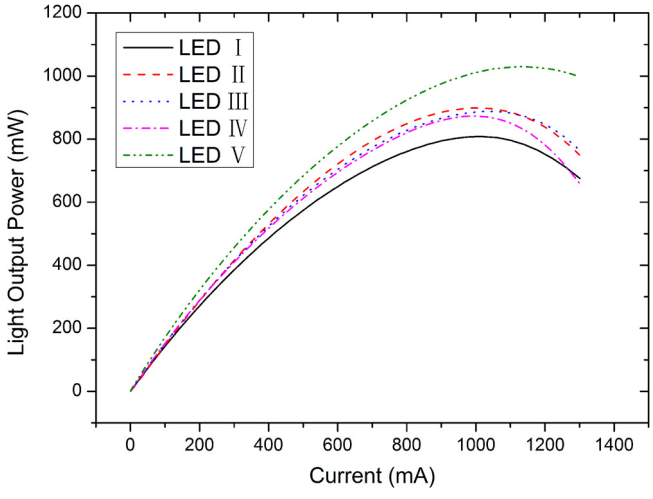

Fig. 7. Light output power of LEDs with different structure.

To further investigate the principle of the LEE improvement by air voids structure, we used a ray tracing software (TracePro) to simulate light propagation in the LED chip. The LEE of the air voids embedded LEDs was calculated by using Monte Carlo ray-tracing method. The light absorption loss by the ITO and p-electrode was ignored to simplify the simulation process. Detailed parameters used in the simulation process were listed in Table 1. For the absorption models, different research groups have presented similar models such as 0 μm^{-1}, 1 μm^{-1}, 0 μm^{-1} [13], 2 mm^{-1}, 120 mm^{-1}, 2 mm^{-1} [14], and 5 mm^{-1}, 8 mm^{-1}, 5 mm^{-1} [15]. In this simulation, the absorption coefficients of *n*-GaN, MQW, and *p*-GaN were assumed to be 2 mm^{-1}, 120 mm^{-1}, and 2 mm^{-1}, respectively.

Fig. 9 showed the simulation structure used for the air voids embedded high power LED chip. The shape of the air void structure was assumed to be conical, which wrapped up the cone-shaped PSS. The dimensions of the PSS and air voids structure were determined from the SEM images shown in Fig. 5. The LED chip size, substrate thickness, and epitaxial layer thickness were 1000 $\mu m \times 1000$ μm, 90 μm, and 6.7 μm, respectively.

Fig. 10 showed the LEE of the air voids embedded LEDs simulated by using Monte Carlo ray-tracing method. In the simulation process, we used 600,000 light rays randomly emitted from the MQW active region layer of LED chip and collected by an integrating sphere. For each ray, the trajectory and the energy were determined by Snell's law, Fresnel losses and material absorption [13]. The LEE of the LED I, LED II, LED III, and LED IV were 30.7%, 38.5%, 38.2%, and 37.8%, respectively. It was found that the LEE of the air voids embedded high power LEDs (LED II, LED III, and LED IV) were all significantly larger than that of the PSS-LED (LED I). The LEE of the air voids embedded high power LED was decreased from 38.5% to 37.8% when the height of air voids structure was increased from 3 μm to 4.8 μm. The simulation results were in good agreement with the experimental results obtained from Fig. 7.

Table 1
Detailed parameters used in the simulation process.

Materials	Refractive index	Absorption coefficient
Sapphire	1.78	0
n-GaN	2.42	2 mm^{-1}
MQW	2.54	120 mm^{-1}
p-GaN	2.45	2 mm^{-1}
ITO	1.95	0

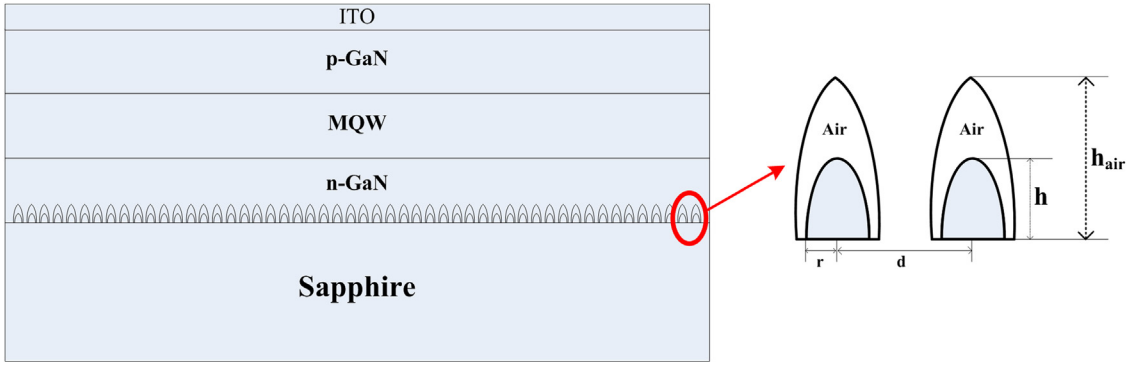

Fig. 9. Simulation structure for the air voids embedded high power LED.

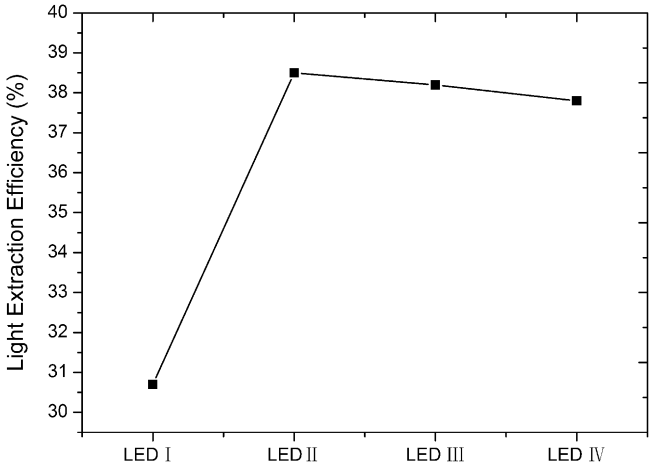

Fig. 10. Simulated light extraction efficiency of LEDs by the TracePro software.

4. Conclusions

Air voids structure was embedded between PSS and GaN epitaxial layer by combining laser scribing with H_3PO_4-based hot chemical etching to improve the LEE of the high power LED, and SiO_2 CBL underneath the p-electrode pad was utilized to improve the current spreading performance of the high power LED. The light output power of the high power LED with embedded air void structure and SiO_2 CBL was 18% higher than that of the conventional PSS-LED.

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