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Highly efficient and reliable high power LEDs with patterned sapphire substrate and strip-shaped distributed current blocking layer

Shengjun Zhou[a,b], Shu Yuan[d], Yingce Liu[d], L. Jay Guo[c], Sheng Liu[a,*], Han Ding[b]

[a] School of Power and Mechanical Engineering, Wuhan University, Wuhan 430072, China
[b] State Key Laboratory of Mechanical System and Vibration, School of Mechanical Engineering, Shanghai Jiao Tong University, Shanghai 200240, China
[c] Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109, USA
[d] Quantum Wafer Inc., Foshan 528251, China

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ABSTRACT

We demonstrated that the improvement in optical and electrical performance of high power LEDs was achieved using cone-shaped patterned sapphire substrate (PSS) and strip-shaped SiO_2 distributed current blocking layer (DCBL). We found through transmission electron microscopy (TEM) observation that densities of both the screw dislocation and edge dislocation existing in GaN epitaxial layer grown on PSS were much less than that of GaN epitaxial layer grown on flat sapphire substrate (FSS). Compared to LED grown on FSS, LED grown on PSS showed higher sub-threshold forward-bias voltage and lower reverse leakage current, resulting in an enhancement in device reliability. We also designed a strip-shaped SiO_2 DCBL beneath a strip-shaped p-electrode, which prevents the current from being concentrated on regions immediately adjacent the strip-shaped p-electrode, thereby facilitating uniform current spreading into the active region. By implementing strip-shaped SiO_2 DCBL, light output power of high power PSS-LED chip could be further increased by 13%.

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1. Introduction

Development on the GaN-based blue LEDs has continued steadily since its invention [1–4]. The white-light sources based on InGaN/GaN multi quantum well (MQW) blue LED chip with phosphor coatings are the most promising solid-state lighting devices, which are slowly pushing aside incandescent and fluorescent lighting [5,6]. Despite significant progress in recent years, the external quantum efficiency (EQE) of LED, which is defined as product of the internal quantum efficiency (IQE) and the light extraction efficiency (LEE), is still required to be further improved [7,8]. Furthermore, larger LED chip area and higher injection current are critical factors yet to be best optimized for achieving higher luminous efficiency [9].

The InGaN/GaN MQW LED was typically grown on heterogeneous sapphire substrate. There are high density defects such as threading dislocations existing in GaN epitaxial layer due to large mismatch in lattice constant and thermal expansion coefficient between the GaN and the sapphire substrate. The use of micro/nano-structure PSS to improve crystal quality of GaN epitaxial layer has been reported [10,11]. Although a few different types of patterns, including grooved, hemispherical, conic, and hexagonal, have recently been proposed for PSS technology [12–15], there has rarely been research into understanding how defect generates and strain relaxes in GaN grown on PSS. Better understanding of defect generation and strain relaxation is extremely crucial to improve optical and electrical performance of LEDs.

In addition, a general requirement of top-emitting LEDs is that both n- and p-type electrodes are formed on the same side of LEDs due to an insulating property of sapphire substrate. Current crowding effect (CCE) around both the p-electrode and the n-electrode emerges in the top-emitting LEDs, degrading device performance [16]. Most scientific efforts have therefore focused on approach to improve current spreading performance of top-emitting LEDs by forming SiO_2 insulating layer underneath the p-electrode pad as a current blocking layer [17,18]. These studies succeeded in improving the current spreading performance of small size LED chip with low input power. However, there are few studies focusing on the design of effective current spreader to improve current spreading performance of size scalable high power LED chip (1–3 W electric power into a LED device of 1 mm^2 area).

* Corresponding author.
E-mail address: victor_liu63@126.com (S. Liu)

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Although the strip-shaped or interdigitated electrodes have been used to improve current spreading performance of high power LED, current crowding around the p-electrode is still severe because the sheet resistance of indium tin oxide (ITO) transparent conductive layer is higher than that of n-GaN layer. To unlock the full potential of high power LED chip, it is imperative to find solutions for effective current spreading when high power LED chip is operated at high driving currents.

Here, we proposed and demonstrated highly efficient high power LED with cone-shaped PSS and strip-shaped distributed current blocking layer (DCBL). The type, distribution and the density of defects existing in GaN epitaxial layer were investigated in detail using scanning electron microscope (SEM), transmission electron microscope (TEM), and high-resolution X-ray diffraction (XRD). Furthermore, a strip-shaped SiO_2 DCBL located below strip-shaped p-electrode was designed to improve current spreading performance over the total light emission area and to enhance uniformity of light emission.

2. Device fabrication

A thermally reflowed photoresist technique and successive BCl_3-based inductively coupled plasma (ICP) etching process were employed to fabricate micro-scale cone-shaped PSS. The detailed fabrication process for cone-shaped PSS has been presented in the previous studies [19]. GaN-based LED epitaxial structure was respectively grown on the conventional FSS (Denoted as FSS-LED) and the cone-shaped PSS (Denoted as PSS-LED) by metal-organic chemical vapor deposition (MOCVD) equipment. Trimethylgallium (TMGa), trimethylindium (TMIn), and ammonia (NH_3) were used as precursors. Silane (SiH_4) and biscyclopentadienymagnesium (Cp_2Mg) were used as the n-dopant and p-dopant source. These LED samples consist of a 30-nm-thick GaN nucleation layer, a 1.5-μm-thick undoped GaN buffer layer, a 2.15-μm-thick Si-doped n-GaN layer, a InGaN/GaN multiple quantum well (MQW), a 100-nm-thick Mg doped p-AlGaN electron blocking layer, and a 190-nm-thick Mg-doped p-GaN layer. The InGaN/GaN MQW structure consists of twelve pairs of 3-nm-thick $In_{0.16}Ga_{0.84}N$ well layers and 12-nm-thick GaN barrier layer. After GaN epitaxial growth process is completed, the LED wafer was subsequently annealed at 750 °C in N_2 atmosphere to activate Mg in the p-GaN layer.

For LED chip fabrication, ICP etching process with BCl_3/Cl_2 gas chemistry was employed to etch GaN MESA structure by removing a portion of p-GaN layer and MQW active layer in order to expose n-GaN layer; a 190-nm-thick strip-shaped SiO_2 DCBL was subsequently formed on the p-GaN surface by plasma enhanced chemical vapor deposition (PECVD) and successive photolithography process; a 112-nm-thick ITO was deposited on the top of p-GaN layer using electronic beam evaporator; the LED wafer with deposited ITO was then rapidly thermal annealed at 540 °C for 10 min in N_2 atmosphere to improve Ohmic contact performance between the ITO and the p-GaN layer; a strip-shaped Cr/Pt/Au (20 nm/50 nm/1.5 μm) was deposited on p-GaN and n-GaN surface as p-electrode and n-electrode, respectively; and the strip-shaped Cr/Pt/Au electrode was aligned with the strip-shaped SiO_2 DCBL; the LED wafer was thinned down to be about 150-μm-thick by mechanical grinding and polishing; finally, the LED wafer was diced into chips with size of 1 mm × 1 mm. The optical and electrical characteristics of high power LEDs were measured by using a probe station system [20].

3. Characterization of threading dislocation

Two effects are responsible for improving luminous efficiency of LED using PSS technology, namely, (i) improved light extraction efficiency of LED due to the angled facets that redirect light into the escape cone, and (ii) enhanced internal quantum efficiency of LED by reducing threading dislocation density, thereby decreasing the concentration of non-radiative recombination centers. The first effect has been extensively explained in previous research efforts by theoretical simulation and experimental verification [21–23]. To explain the second effect, TEM and high-resolution XRD were used to thoroughly investigate the type, the distribution and the density of defects existing in GaN layer grown on PSS and FSS in this research.

Here we employed XRD rocking curves method to evaluate crystal quality of GaN grown on FSS and PSS, respectively. The FWHM of the symmetry (0 0 2) rocking curves of GaN grown on FSS and PSS were 300″ and 249″, respectively. The FWHM of the asymmetry (1 0 2) rocking curves of GaN grown on FSS and PSS were 310″ and 270″, respectively. It was reported that the X-ray *w*-scan curves on the symmetric (0 0 2) planes and asymmetric (1 0 2) planes were mainly influenced by screw type and edge type dislocations, respectively [14]. The density of threading dislocation can be estimated from the full width at half maximum (FWHM) of GaN (0 0 2) and GaN (1 0 2) using the following equation [24]:

$$N = \frac{\beta^2}{4.35|b|^2} \tag{1}$$

where N is the dislocation density, $|b|$ is the magnitude of the Burgers vector, and β is the FWHM of the X-ray rocking curve. The calculated densities of screw dislocation were $1.88 \times 10^8\ \text{cm}^{-2}$ and $1.29 \times 10^8\ \text{cm}^{-2}$ for GaN grown on FSS and PSS, respectively; the calculated densities of edge dislocation were respectively $5.4 \times 10^8\ \text{cm}^{-2}$ and $4.1 \times 10^8\ \text{cm}^{-2}$ for GaN grown on FSS and PSS according to Eq. (1). In addition, cross-check of the results obtained by XRD was conducted using plan-view TEM images.

Using bright filed and dark field TEM analyses, we carried out a comparative study of the defect properties existing in GaN grown on FSS and PSS, respectively. Fig. 1(a) showed the bright field TEM image of GaN grown on FSS. It was revealed from Fig. 1(a) that GaN grown on FSS contained three different types of threading dislocations: edge, screw, and mixed. The GaN grown on FSS is typically under compressive strain because of large lattice mismatch [25]. Under the compressive stress condition, the Frank–Read source, which multiplies in a two-dimensional direction, can spiral many times, thereby generating dislocation loops in a wider range, which further degrades crystal quality [13,26]. This was consistent with Fig. 1(a) where some dislocation loops near the GaN/FSS interface, a typical Frank–Read source multiplication area, were observed in GaN grown on FSS case. Weak beam dark field TEM image of GaN grown on FSS was illustrated in Fig. 1(b) and (c), respectively. The edge and screw dislocations have Burgers vectors ($\mathbf{b_e} = \langle 1\,1\,\bar{2}\,0\rangle$ and $\mathbf{b_s} = \langle 0\,0\,0\,1\rangle$, respectively) [27]. In Fig. 1(b), only the screw and mixed dislocations were visible. In Fig. 1(c), only edge and mixed dislocations were visible.

For comparison, Fig. 1(d) showed the bright filed TEM image of GaN grown on PSS. Because of the fewer Frank-Read source multiplications, GaN grown on PSS case is of lower dislocation density as shown in Fig. 1(d). Instead of dislocation loops, threading dislocations, which climb in a one-dimensional direction and have an impact on crystal quality in a smaller range, emerge in GaN grown on PSS due to the relaxation of compressive strain caused by the surface geometry of PSS [28]. Weak beam TEM image of GaN grown on PSS demonstrating screw and mixed dislocations was shown in Fig. 1(e). Weak beam TEM image of GaN grown on PSS demonstrating edge and mixed dislocations was shown in Fig. 1(f). In contrast to the weak beam dark field TEM image of GaN grown on FSS, we found that densities of the edge, screw and mixed dislocations of GaN grown on PSS were remarkably less than that of GaN grown on FSS.

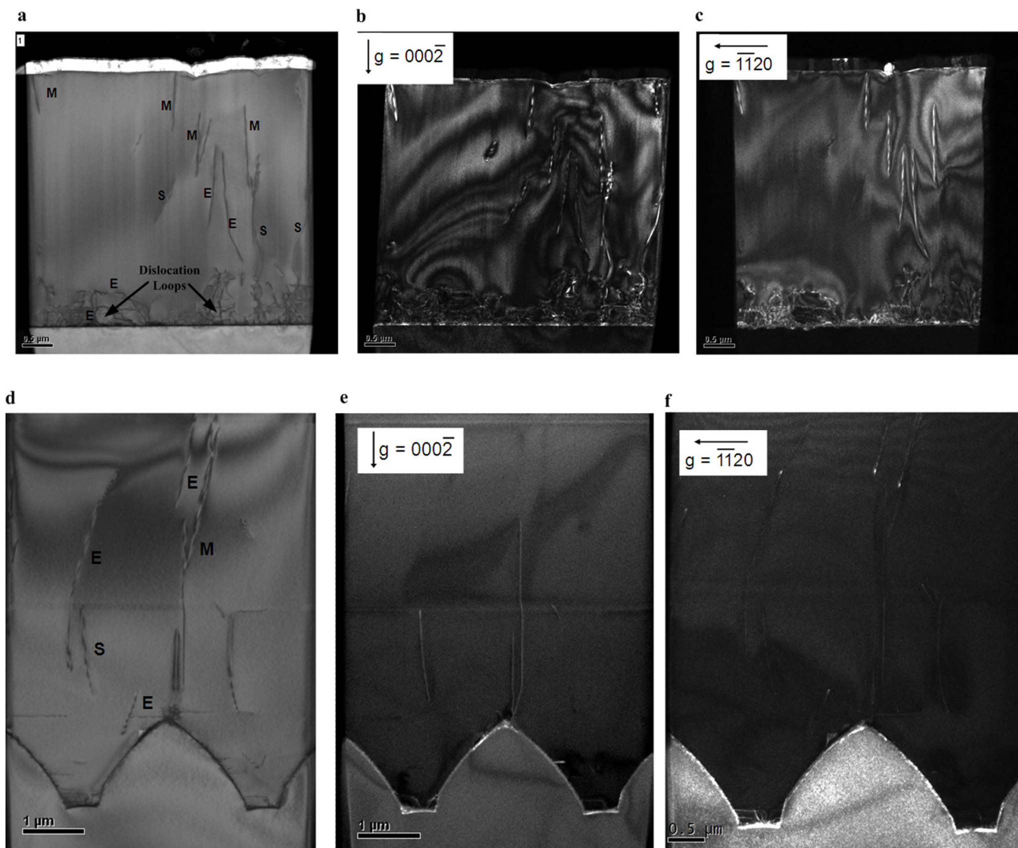

Fig. 1. TEM images of GaN epitaxial layer gown on FSS and PSS. (a) Cross-sectional bright field TEM image of GaN grown on FSS. (b) Weak beam TEM image of GaN grown on FSS demonstrating screw and mixed dislocations. g is the reciprocal lattice vector, and the arrows indicate the direction of the vectors. The numbers are Miller indices. (c) Weak beam TEM image of GaN grown on FSS demonstrating edge and mixed dislocations. (d) Cross-sectional bright field TEM image of GaN grown on PSS. (e) Weak beam TEM image of GaN grown on PSS demonstrating screw and mixed dislocations. (f) Weak beam TEM image of GaN grown on PSS demonstrating edge and mixed dislocations.

The structural properties of InGaN/GaN MQW, which were respectively grown on FSS and PSS, were further investigated by high-resolution TEM imaging. Fig. 2(a) showed the TEM image of InGaN/GaN MQW grown on FSS. Fig. 2(b) showed TEM image of InGaN/GaN MQW grown on PSS. By comparing Fig. 2(b) with Fig. 2(a), it was revealed that crystal quality of InGaN/GaN MQW grown on PSS was much better than that of InGaN/GaN MQW grown on FSS. In the vicinity of threading dislocation, a V-shaped pit with sidewall QW appeared and the formation of V-shaped pit exactly corresponded with the surface termination of threading dislocations as shown in Fig. 2(b). Hangleiter et al. reported that the V-shaped pits decorating every threading dislocation could be the mechanism of high emission efficiency in InGaN/GaN MQW LEDs [29]. Fig. 2(c) showed the STEM-BF lattice image illustrating lattice fringes from GaN barrier layer. The lattice spacing between the adjacent planes was measured to be 0.51 nm, corresponding to the *d*-spacing of (0 0 0 1) plane of wurtzite GaN crystal structure.

The electrical performance of LEDs were characterized in terms of five critical points, namely forward voltage one (VF1), forward voltage two (VF2), forward voltage three (VF3), forward voltage four (VF4), and reverse leakage current (IR), which were respectively specified at operating current (@350 mA), a small forward current (@10 μA), a small forward current (@5 μA), a very small

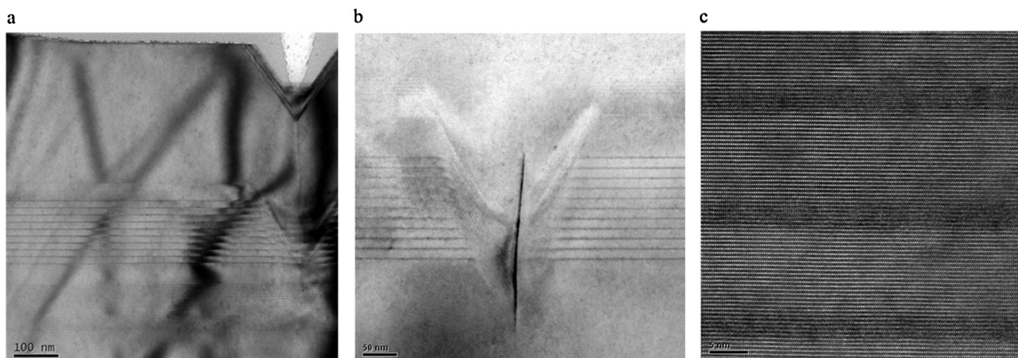

Fig. 2. TEM images of InGaN/GaN MQW grown on FSS and PSS. (a) High resolution TEM image of InGaN/GaN MQW grown on FSS. (b) High resolution TEM image of InGaN/GaN MQW grown on PSS. The presence of V-shaped pits is clearly observed in the InGaN/GaN MQW structure. (c) STEM-BF lattice image illustrating lattice fringes from GaN barrier layer.

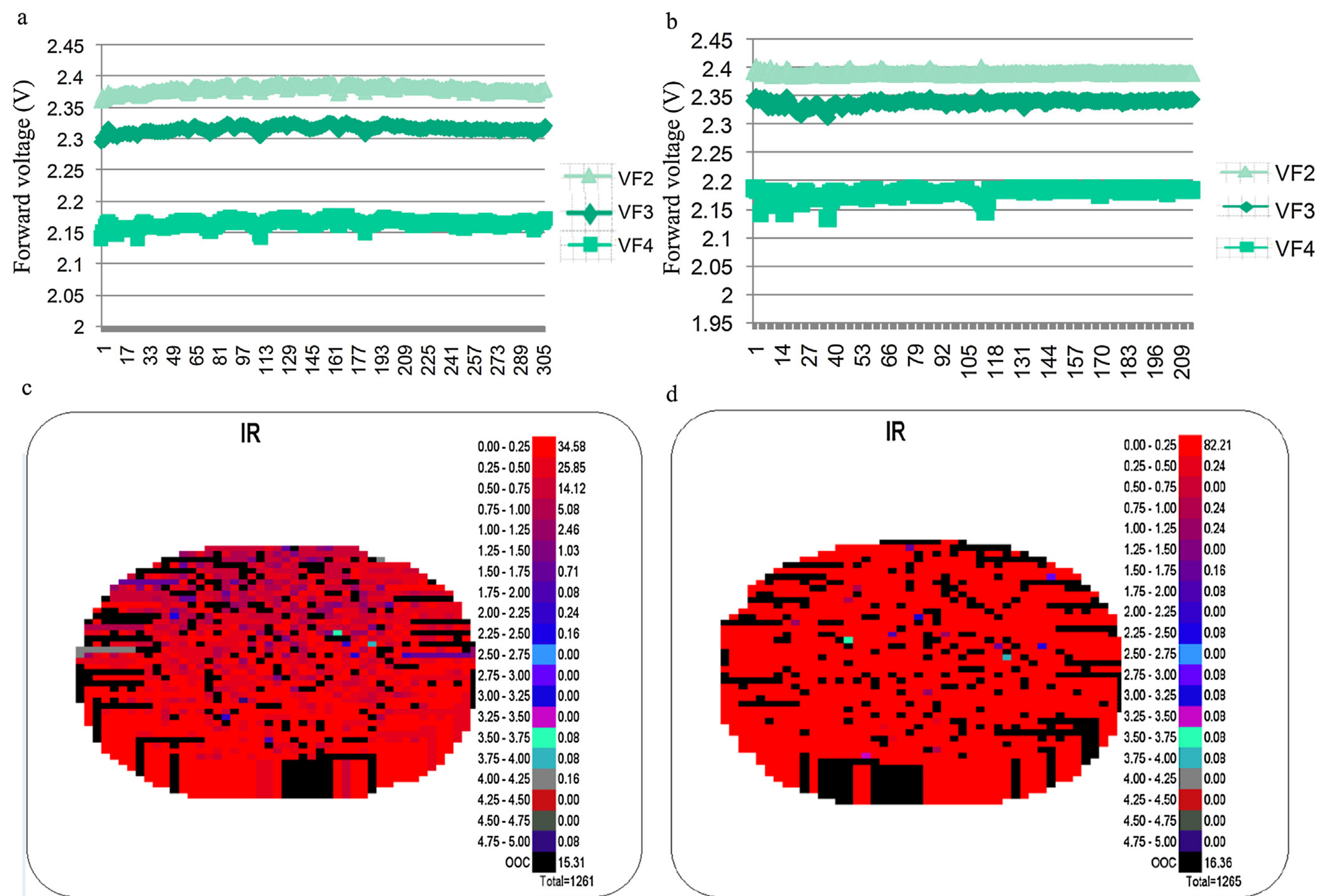

Fig. 3. Measured forward voltage and reverse leakage current. (a) Forward voltage of LED chip in a wafer grown on FSS. The VF2, VF3, and VF4 are measured under a driven current of 10 μA, 5 μA, and 1 μA, respectively. (b) Forward voltage of LED in a wafer grown on PSS. (c) Distribution of reverse leakage current in a LED wafer grown on FSS. (d) Distribution of reverse leakage current in a LED wafer grown on PSS.

forward current (@1 μA), and at negative bias (@−7 V). The values of sub-threshold forward-bias voltage, including VF2, VF3 and VF4, each of which is well correlated with crystal growth quality and device reliability, should be as high as possible because low values of sub-threshold forward-bias voltage indicate excessive sub-threshold leakage [30]. The reverse leakage current, which is well correlated with device reliability, lifetime, and degradation under high power operating condition, should be as low as possible because high value of reverse leakage current indicates excessive leakage paths caused by high densities of screw and mixed dislocation [31–33].

In order to quantitatively analyze the relationship between the dislocation density and the reverse leakage current and also the LED performance, the effect of dislocation density on sub-threshold forward-bias voltage and reverse leakage current of LEDs was analyzed. For LED grown on FSS (FSS-LED) with high dislocation density, the values of sub-threshold forward-bias voltage, including VF2, VF3 and VF4, were 2.36 V (@10 μA), 2.31 V (@5 μA), and 2.15 V (@1 μA), respectively as shown in Fig. 3(a). For LED grown on cone-shaped PSS (PSS-LED) with low dislocation density, the values of sub-threshold forward-bias voltage, including VF2, VF3 and VF4, were 2.40 V (@10 μA), 2.35 V (@5 μA), and 2.19 V (@1 μA), respectively as shown in Fig. 3(b). Compared to FSS-LED, the observed higher sub-threshold forward-bias voltage in PSS-LED is attributed to the reduction in densities of defects, leading to a decrease in defect-assisted tunneling process.

Fig. 3(c) showed reverse leakage current distribution of FSS-LED chips in a wafer. As shown in Fig. 3(c), 34.5% of FSS-LED chips in a wafer have value of reverse leakage current less than 0.25 μA. Fig. 3(d) showed reverse leakage current distribution of PSS-LED chips in a wafer. As shown in Fig. 3(d), 82.2% of PSS-LED chips in a wafer have value of reverse leakage current less than 0.25 μA. In other words, the average value of reverse leakage current in PSS-LED chips with low dislocation density was less than that of reverse leakage current in FSS-LED chips with high dislocation density.

Table 1
Measured change in resistivity of grown n-GaN with different n-doped Si concentration.

Sample no.	Resistivity (Ω cm)	Carrier mobility ($cm^2/V^{-1} s^{-1}$)	Carrier density (cm^{-3})
1	0.005374	223	−5.428E+18
2	0.004815	218	−5.948E+18
3	0.004697	203	−6.544E+18
4	0.004582	191	−7.147E+18

In order to quantitatively analyze the relationship between the reverse leakage current and the LED performance, the degradation of blue PSS-LED with low reverse leakage current and blue FSS-LED with high reverse leakage current was investigated based on high temperature operation life test. The PSS-LED and FSS-LED samples were placed in a thermal chamber that is controllable from room temperature to 100 °C, and LED samples were then stressed at the condition of 85 °C using an injection current of 350 mA. The blue PSS-LED and FSS-LED samples were removed from the thermal chamber at specific intervals to measure their light output power. The normalized light output power degradation of PSS-LED

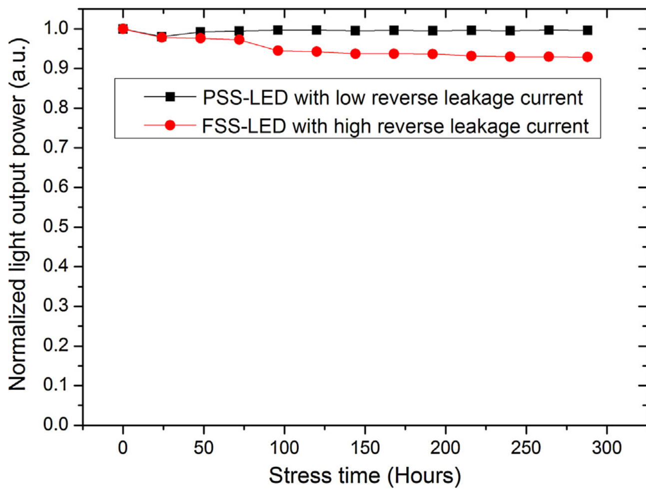

Fig. 4. Normalized light output power degradation of LED during high temperature operation life test process.

and FSS-LED was shown in Fig. 4. After high temperature operation life test (288 h), the light output power of PSS-LED decreased by 0.41%, while the light output power of FSS-LED decreased by 7.01%. Compared to the FSS-LED with high reverse leakage current, the PSS-LED with low reverse leakage current exhibited markedly smaller optical degradation and thus higher device reliability.

4. Design and fabrication of strip-shaped SiO_2 DCBL

Current spreads laterally in top-emitting GaN-based LEDs. The current density $J(x)$ extends away from the electrical contact based on the current spreading theory, which can be expressed as [34,35]

$$J(x) = J_0 \exp\left(\frac{-x}{L_s}\right) \tag{2}$$

where J_0 is the maximum current density at the electrode edge, x is the distance from a certain location to the electrode edge and L_s is denoted as the current spreading length, which is related to J_0 and sheet resistance of ITO and n-GaN layer. L_s, usually used to evaluate the current crowding effect (CCE), can be expressed as [36,37]

$$L_s = \sqrt{\frac{2n_{ideal}kT/q}{J_0(\rho_{s,\mathrm{ITO}} + \rho_{s,\mathrm{n\text{-}GaN}})}} \tag{3}$$

where $\rho_{s,\mathrm{ITO}}$ and $\rho_{s,\mathrm{n\text{-}GaN}}$ are sheet resistances of ITO and n-GaN layer, respectively. k, q and T are the Boltzmann constant, element charge, and temperature, respectively. n_{ideal} is the ideality factor of GaN-based LEDs. In this paper, the n_{ideal} is assumed to be 5.

Fig. 5 showed the measured sheet resistance and transmittance of ITO transparent conductive layer. The measured sheet resistance of ITO is about 48 Ω/□ when the thickness of ITO is fixed at 112 nm. The transmittance of 112-nm-thick ITO is higher than 95% for blue light wavelength region after thermal annealing, which makes ITO excellent performance for blue high power LED chip.

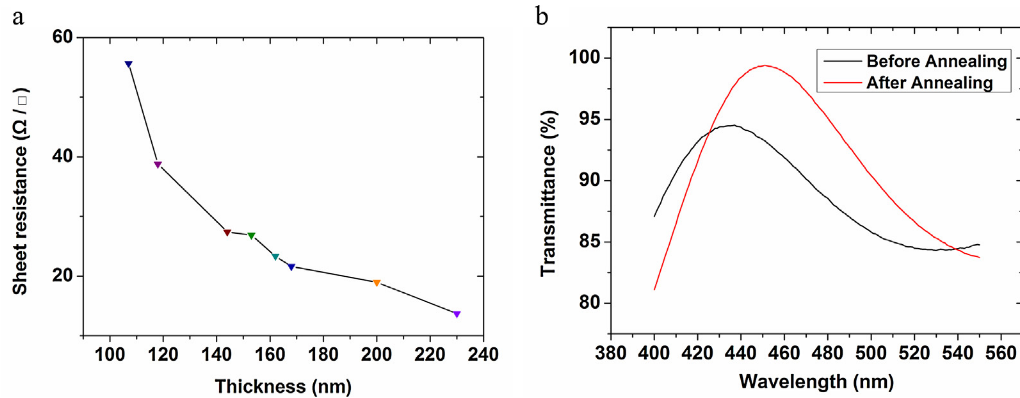

Fig. 5. Measured sheet resistance and transmittance of ITO transparent conductive layer. (a) Measured change in sheet resistance when the ITO with different thicknesses is deposited on silicon with thermally oxide silicon dioxide. (b) Measured change in transmission spectra of a 112-nm-thick ITO deposited on quartz before and after thermal annealing.

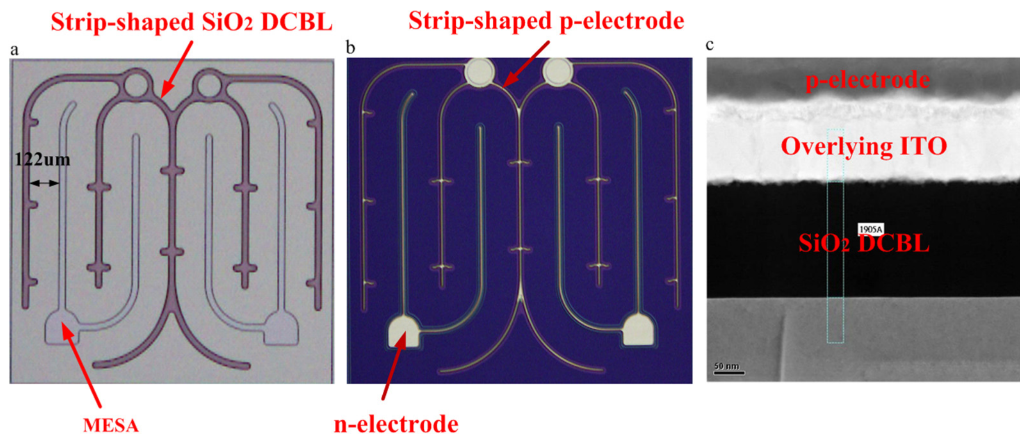

Fig. 6. Demonstration of the strip-shaped SiO_2 DCBL and the strip-shaped p-electrode. (a) Optical image of the strip-shaped SiO_2 DCBL and the etched MESA. Pink section in the image is the strip-shaped SiO_2 DCBL. (b) Optical image of the electrode pattern demonstrating the strip-shaped Cr/Pt/Au metallic electrode, which located on the top of strip-shaped SiO_2 DCBL. (c) TEM image of the deposited multilayer thin films, including SiO_2 DCBL, ITO and Cr/Pt/Au.

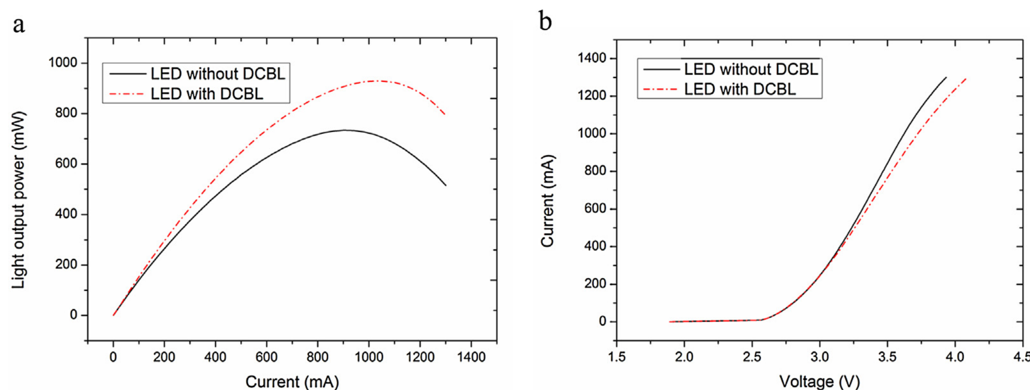

Fig. 7. Light output power and forward voltage one (VF1) of high power PSS-LED versus injection current. (a) Light output power of high power PSS-LED versus injection current. (b) Forward voltage of high power PSS-LED versus injection current.

The resistivity of grown n-GaN layer depends on the carrier concentration. The measured change in resistivity of n-GaN layer with different carrier density was shown in Table 1. The sheet resistance of grown n-GaN layer is 21.8 Ω/□ when the carrier density of n-GaN layer and the thickness of n-GaN layer are 6.544E+18 and 2.15 μm, respectively. Electron mobility decreased with increasing carrier density due to the higher rate of carrier-carrier scattering at higher carrier density.

The current crowding around p-electrode emerged because the sheet resistance of 112-nm-thick ITO transparent conductive layer (48 Ω/□) was much higher than that of grown n-GaN layer (21.8 Ω/□). Therefore, we designed a strip-shaped SiO_2 DCBL underneath a strip-shaped p-electrode pattern in order to alleviate the current crowding around the p-electrode and to increase light output power of PSS-LED. The fabricated strip-shaped SiO_2 DCBL was shown in Fig. 6(a). The distance between the strip-shaped finger of SiO_2 DCBL structure and the edge of etched MESA structure was determined according to the calculated L_s. The L_s is estimated to be about 122.3 μm when the sheet resistance of ITO and n-GaN layer is 48 Ω/□ and 21.8 Ω/□, respectively. Hence, the distance between the strip-shaped finger of SiO_2 DCBL structure and the edge of etched MESA structure is designed to be 122 μm, as shown in Fig. 6(a). Fig. 6(b) showed the overlying strip-shaped p-electrode pattern, which was deposited on the top of strip-shaped SiO_2 DCBL. The diameter of bonding electrode (p-electrode pad) is 100 μm, whereas the diameter of SiO_2 DCBL is 113 μm. The diameter of bonding electrode is set to be smaller than that of the DCBL. The width of strip-shaped SiO_2 DCBL is 25 μm, and the width of overlying strip-shaped p-electrode is 7 μm. Fig. 6(c) showed the TEM image of deposited multilayer thin films, including 190-nm-thick SiO_2 DCBL, 112-nm-thick ITO, and Cr/Pt/Au p-electrode. Because the ITO located below the p-electrode extended beyond the perimeter of p-electrode, the SiO_2 DCBL underneath the ITO transparent conductive layer prevent injection current from being concentrated on regions immediately adjacent the p-electrode of PSS-LED where any light emitted would be absorbed by the opaque p-electrode. Furthermore, the current propagation along the lateral direction of ITO transparent conductive layer being much larger than its perpendicular direction, the strip-shaped SiO_2 DCBL is therefore likely to ease out the heat from the high power PSS-LED chip by acting as a current spreader.

Fig. 7 showed light output power and forward voltage one (VF1) of the fabricated high power PSS-LEDs as a function of injection current. At 350 mA injection current, the light output powers of PSS-LED without SiO_2 DCBL and PSS-LED with SiO_2 DCBL were 430 mW and 486 mW, respectively; and the VF1 of PSS-LED without DCBL and PSS-LED with DCBL were 3.10 V and 3.11 V, respectively. In contrast to PSS-LED without SiO_2 DCBL, a slightly increased forward voltage one (VF1) of 0.01 V for PSS-LED with SiO_2 DCBL was observed, which can be attributed to a reduction in the total area of the p-type Ohmic contact between the ITO and the p-GaN layer due to the presence of insulating SiO_2 DCBL, leading to an increase in resistance of current path. Light output power of the PSS-LED with SiO_2 DCBL was approximately 13% higher than that of the PSS-LED without SiO_2 DCBL. Accordingly, significantly increased luminous efficiency for high power PSS-LED chip can be achieved by employing strip-shaped SiO_2 DCBL.

5. Conclusions

In conclusion, we found that densities of the edge, screw and mixed dislocation of PSS-LED were less than that of the FSS-LED. In contrast to FSS-LED, the forward voltage two (VF2) of PSS-LED operated at a small forward current (@10 μA) was higher, whereas the reverse leakage current (IR) of PSS-LED operated at negative bias (@−7 V) was lower due to a reduction in densities of threading dislocations, leading to an enhancement in device reliability. By implementing strip-shaped SiO_2 DCBL, we demonstrated approximately 13% higher light output power for high power PSS-LED chip. The strip-shaped SiO_2 DCBL located below strip-shaped p-electrode can prevent current from being concentrated on regions immediately adjacent the p-electrode where the overlying p-electrode metal layer would absorb the emitted light. Furthermore, current flow is directed to other portions of active layer, thereby increasing the luminous efficiency of high power PSS-LED.

Acknowledgements

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