CHAPTER 8

Semiconductor Nanowires for Electronic and Optoelectronic Device Applications

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1. INTRODUCTION

With the discovery of carbon nanotubes in 1991 [1], nanoscale materials have attracted tremendous interest and attention over the past decade for their vast areas of applications ranging from electronics to pharmaceuticals. Nanostructures are defined as having dimension between 1 to 100 nm. One-dimensional (1D) nanostructures such as nanowires, nanobelts

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and nanotubes have become the focus of intensive research owing to their fascinating properties, unique applications in mesoscopic physics and fabrication of nanoscale electronic and optoelectronic devices. Controllable synthesis of nanomaterials to achieve 1D nanostructures with desirable morphology and anisotropic growth is critical to attain unique properties for the realization of potential nanoscale electronic and optoelectronic multifunctional devices.

Semiconductor nanowires have demonstrated significant potential as fundamental building blocks for nanoelectronic and nanophotonic devices and offer substantial promises for integrated nanosystems. The rectifying properties of semiconductor nanowires-based electronics demonstrated the versatility of the nanowires-based electronics device. Quantum confinement effects of the semiconductor nanowires on the other hand, produce unique optical properties that can be applied to nanophotonic devices. Notably, the key feature of semiconductor nanowires that has enabled much of their success has been the growth of materials with reproducible electronic and optical properties that can be in turn, integrated into functional nanoscale devices. Consequently, nanodevices based on semiconductor materials such as nano-field-effect transistors (FETs) [2], nano-lasers [3], nano-light emitting diodes (LEDs) [4] and nanosensors [5] have been demonstrated. To date, many semiconductor nanowires have been successfully fabricated by various techniques. Currently, there exist substantial limitations on the use of nanowires or nanotubes for integrated nanoelectronics or even simple device arrays as current development of the assembly techniques still lacks controllability and reproducibility. In this chapter, a review of some principal synthesis methods for the growth of single crystalline semiconductor nanowires will be illustrated. A highlight on the range of unique properties associated with the semiconductor nanowires as well as their potential electronic and optoelectronic device applications will also be discussed. And lastly, the efforts in developing some of the assembly techniques for the nanowires arrays for integrated nanosystems will also be evaluated.

2. SYNTHESIS OF SEMICONDUCTOR NANOWIRES

Recently nanotubes or nanowires from a wide variety of inorganic semiconductor materials have been successfully synthesized by various established approaches. These include chemical vapor deposition, metal-catalyzed growth assisted by laser, solution-liquid-solution methods, vapor phase growth, oxide-assisted growth, metal-organic chemical vapor deposition (MOCVD), template-confined growth, solvothermal methods, and more. For simplicity, some of the above-mentioned approaches are categorized under catalytic growth or non-catalytic growth methods in this chapter. A review of the established synthesis methods for semiconductor nanowires will be discussed in this section.

2.1. Catalytic Methods via Vapor-Liquid-Solid Growth Mechanism

Wagner and Ellis [6] identified a vapor-liquid-solid (VLS) growth mechanism for single crystal whisker growth in 1964 and provided a clear demonstration of one-dimensional crystal growth due to size confinement of a catalytic cluster solvent medium. The VLS method has become a popular method for the synthesis of 1D semiconductor nanowires and nanotubes that include elemental semiconductors (Si, Ge, B) [7], III–V semiconductors (GaN, GaAs, GaP, InP, InAs) [8], II–VI semiconductors (ZnS, ZnSe, CdS) [9] and oxides (MgO, Ga_2O_3) [10]. Both chemical methods (chemical vapor transport and deposition) and physical methods (laser ablation, thermal evaporation, arc discharge, etc.) are employed to generate vapor species required for the growth of 1D nanowires and nanotubes. The major steps involved in a VLS process are schematically depicted in Fig. 1(a) [11]. A catalyst is first applied to the substrate surface prior to nanowires synthesis. There are a variety of ways of preparing the catalyst and introducing it into the process. The catalyst can be introduced either *in situ* or *ex situ*, depending on the synthesis process. For example, in laser ablation synthesis, the catalyst is introduced directly into the ablation target. This is easily done by mixing powders of the catalyst and nanowires material and then pressing it into a target. While in the case of *ex situ* application, physical vapor deposition techniques such as electron beam evaporation and sputtering can be utilized to deposit a few monolayers of the catalyst onto the

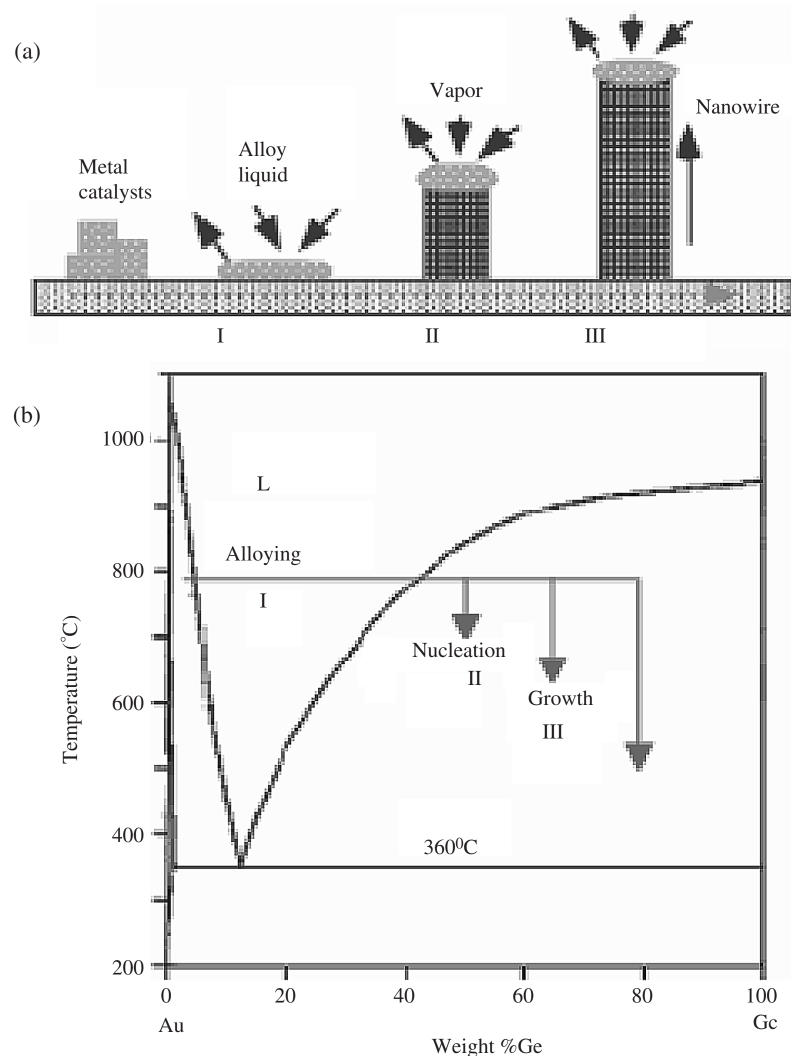


Figure 1. (a) Schematic illustration of Ge nanowires growth by VLS mechanism, including 3 stages (I) alloying, (II) nucleation, and (III) axial growth. The 3 stages are projected onto the conventional Au-Ge binary phase diagram (b) to show the compositional and phase evolution during the nanowires growth process. Reprinted with permission from [11], Y. Wu and P. Yang, *J. Am. Chem. Soc.* 123, 3165 (2001). © 2001, American Chemical Society.

substrate. After catalyst application, vapors of the target material are generated by choosing growth temperature above the melting point of the target material. While the substrate is kept at or above the eutectic temperature of the alloy metal catalyst and target material, this is to ensure that the solid metal catalyst transforms into nanometered size liquid droplets. If the catalyst is not liquid, material in the vapor will not be absorbed, thereby prohibiting nanowires growth. The generated vapors of the target material would then interact and dissolves into the nanometer-sized liquid alloy. As more and more vapor phase materials dissolve into the liquid alloy, it eventually becomes supersaturated and results in the nucleation and growth of single crystalline nanowires on the substrate surface. In the VLS process, the growth of the 1D nanostructures is mainly induced and controlled by the liquid catalyst, therefore an appropriate choice of catalyst must be made. As the ability of the metal catalyst to form a liquid alloy with the vapor species of the target material is crucial in nanowires formation, a metal catalyst should be rationally chosen from the phase diagram [Fig. 1(b)]. By identifying a metal that forms a liquid alloy with the target material vapor at the growth temperature, the liquid alloy serves as the site for adsorbing the incoming molecules. The metal catalyst does not form a solid solution with the nanowires, but is phase separated at the growth front and leads the growth. During the growth, the liquid alloy directs the nanowire's

growth direction and defines the diameter of the nanowires. By controlling the growth temperature and thickness of the metal film, one could control the diameter of the liquid alloy which would eventually dictate the final diameter of the nanowires. Typically, lower growth temperatures and thinner metal film would result in thinner nanowires. As a result solid catalyst nanoparticles at the ends with sizes comparable to the diameters of the connected nanowires are often observed. Wu et al. have confirmed this mechanism by *in-situ* observation of the growth of Ge nanorods in the chamber with the aid of a transmission electron microscope (TEM), equipped with a temperature-controlled stage [11]. Ge nanorods were grown with GeI_2 as the vapor source and Au as catalyst. Based on this mechanism, it was found that the diameter of the size of the nanowires can be controlled by the size of the catalyst. The smaller the catalyst should yield thinner nanowires. However, the major drawback of VLS method is the presence of the catalyst nanoparticles at the ends of the nanowires which may contaminate the semiconductor nanowires and thus altering their properties.

2.1.1. Chemical Vapor Deposition

Chemical vapor deposition (CVD) is a chemical process which transforms one of more volatile gaseous precursor, into a solid material in the form of thin film or powder, on the surface of a substrate. CVD has advantages of variety in products and hydrocarbon sources, adequacy for synthesis of high quality materials, and controllability of microscopic structures. Recently this process is also widely employed to synthesize various semiconductor nanowires including Si [7], ZnO [12], GaN [13], In_2O_3 [14] and etc.

An example of CVD growth of Si nanowires is shown in Fig. 2. Zhang et al. employed the experimental setup depicted in Fig. 2 for the growth of Si nanowires at ambient pressure by using $SiCl_4$ as Si source, Ni film as the catalyst and Al_2O_3 as substrate at 700 °C via chemical vapor deposition process [7]. In this technique, the growth of the Si nanowires with diameters between 10 to 20 nm (Fig. 3), was proceeded by the VLS mechanism, with the Ni/Si dictating the growth and nucleation of the Si nanowires.

2.1.2. Metal-Catalyzed Growth Assisted by Laser Ablation

Duan et al. [15], based on the vapor-liquid-solid growth mechanism have developed a new method to synthesized semiconductor nanowires by laser ablation of a metal-containing target, in which the metal nanoparticles were used as catalyst. His group demonstrated the use of metal catalysts containing target materials for producing several semiconductor nanowires including Si, Ge, GaAs, InP, GaP, and GaN. They followed the scheme illustrated in Fig. 4 for the growth and nucleation of single crystal GaN by laser-assisted catalytic technique. Laser ablation of a composite target (GaN:Fe) generated liquid Fe clusters that serve as the reactive sites confining and directing the growth of the crystalline GaN nanowires.

Lam et al. also demonstrated the VLS growth of single crystalline β-Ga_2O_3 nanowires by pulsed laser ablation technique with the use of Au catalyst as illustrated Fig. 5. A detailed explanation of the experimental setup can be found in [16]. A thin Au layer of ~5 nm

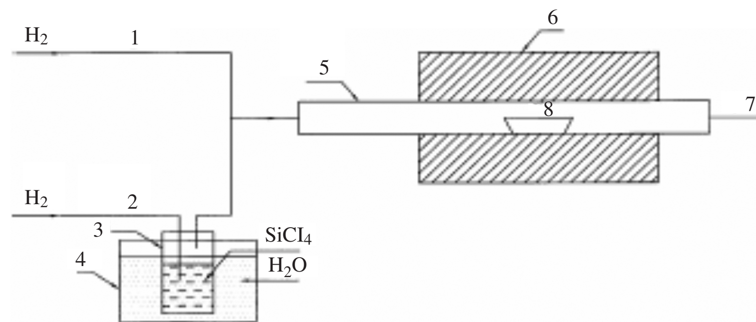


Figure 2. The synthesis system scheme of Si nanowires (1) and (2) H_2 flow, (3) $SiCl_4$ container, (4) water container, (5) quartz tube, (6) furnace, (7) waste gases, (8) Al_2O_3 boat covered by a Ni film inside. Reprinted with permission from [7], Y. J. Zhang et al., *J. Cryst. Growth* 226, 185 (2001). © 2001, Elsevier.

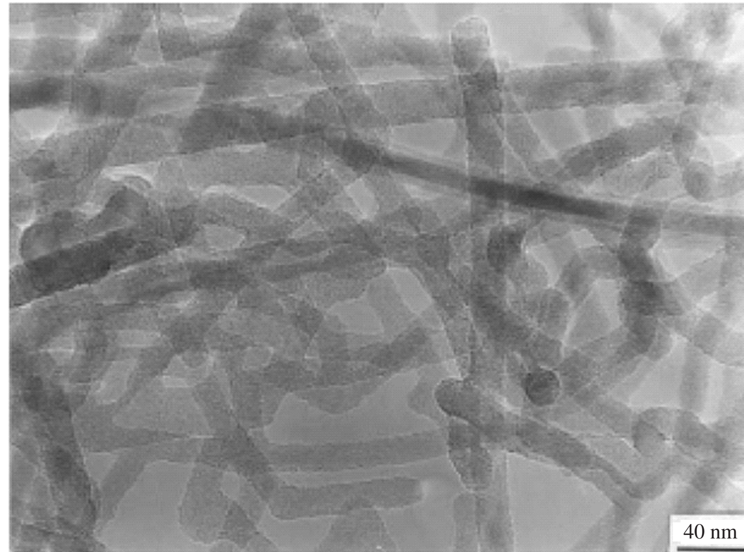


Figure 3. Si nanowires with diameters between 10–20 nm [7].

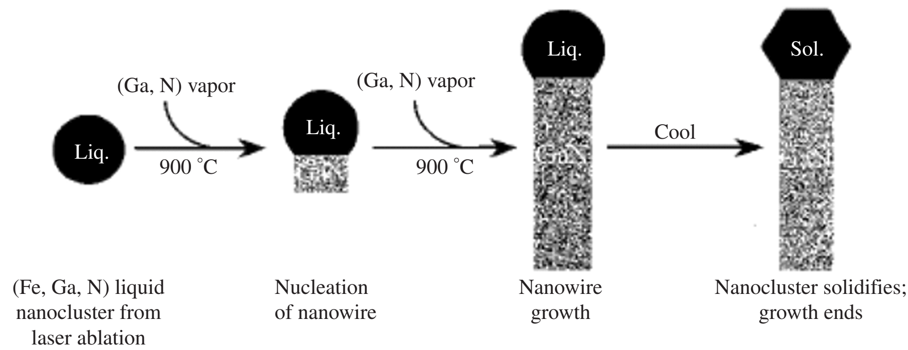


Figure 4. Schematic illustration of the VLS growth of GaN nanowires. Reprinted with permission from [15], X. Duan and C. M. Lieber, *J. Am. Chem. Soc.* 122, 188 (2000). © 2000, American Chemical Society.

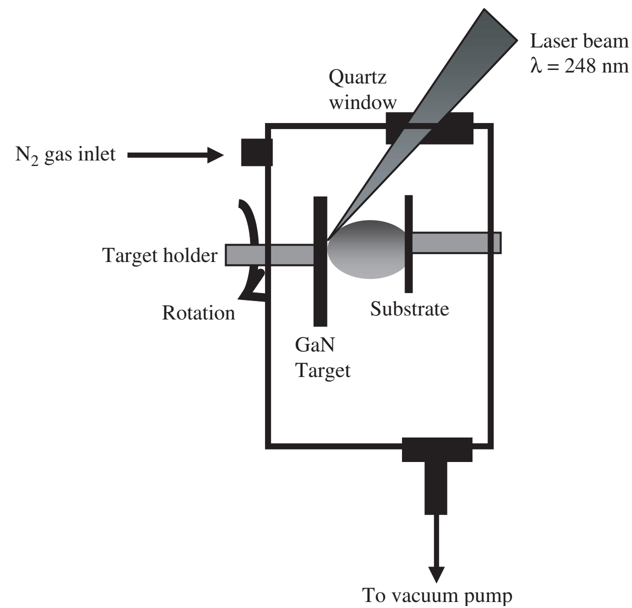
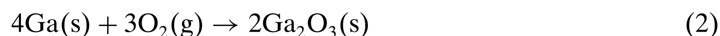


Figure 5. Schematics of β-Ga_2O_3 nanowires synthesis by laser ablation. Reprinted with permission from [16], H. M. Lam et al., *App. Phys. A* 79, 2099 (2004). © 2004, Springer.

was deposited on the Si substrate via e-beam evaporation prior to the nanowires growth. Laser irradiation of the GaN target with KrF excimer laser ($\lambda = 248$ nm) led to the thermal decomposition of GaN. GaN decomposes thermally via the following possible reactions:

$$4GaN(s) \rightarrow 4Ga(l) + 2N_2(g) \quad (1)$$



$$4Ga(s) + 3O_2(g) \rightarrow 2Ga_2O_3(s) \quad (2)$$

Here, the decomposition of GaN proceeds via photochemical laser ablation mechanism. The photon energy of the laser beam of about 4.9 eV is sufficient to break the chemical bonds between gallium and nitrogen that contributes to the supply of Ga vapor. According to the Au/Ga phase diagram (Fig. 6), when the Ga concentration reaches 95%, Au becomes liquid at 700 °C and Ga vapor is able to dissolve into the nanometer-sized liquid Au catalyst [Fig. 7(a)] on the Si substrate. Each Ga-Au nanodroplet acted as a nucleus that is energetically favored to absorb incoming Ga vapor. When the droplets became supersaturated, the metallic Ga precipitated out of the droplet and recombined with oxygen in the chamber to form Ga_2O_3 nanocrystals and further grow epitaxially into nanorods or nanowires. The diameter of the β-Ga_2O_3 nanowires was found to be ~50 nm as ~50 nm as shown in Fig. 7(c). Figure 7(d) shows the high resolution transmission electron microscopy (TEM) image of a metal tip that dictated the subsequently growth and nucleation of the β-Ga_2O_3 nanowires. Energy dispersive spectroscopy (EDX) analysis was carried out to determine composition of the metal tip, it was found to consist of Ga-Au. It is also evident in Fig. 7(d) that the diameter of the nanowires is dictated by the size of the metal nanoparticles as the diameter of the nanowires is comparable to the diameter of the metal nano-tip. Here, the growth of the β-Ga_2O_3 nanowires is attributed by attributed by vapor-solid-liquid mechanism. Figure 8 shows a typical X-ray diffraction (XRD) pattern of the as-deposited nanowires synthesized at 10 Torr chamber pressure and at a laser fluence of 4.25 J/cm^2. The diffraction peaks can be indexed as a monoclinic phase Ga_2O_3 (JCPDS Card 11-0370). The lattice constants calculated from the pattern are $a_0 = 5.80$ Å, $b_0 = 3.04$ Å, $c_0 = 12.23$ Å and $\beta = 103.42°$ for Ga_2O_3. However, the relative intensity is different, for which the strongest peaks of bulk Ga_2O_3 powder are (004), (104), (200), (111) and (122), whereas for β-Ga_2O_3 nanowires, the strongest peak is only (113).

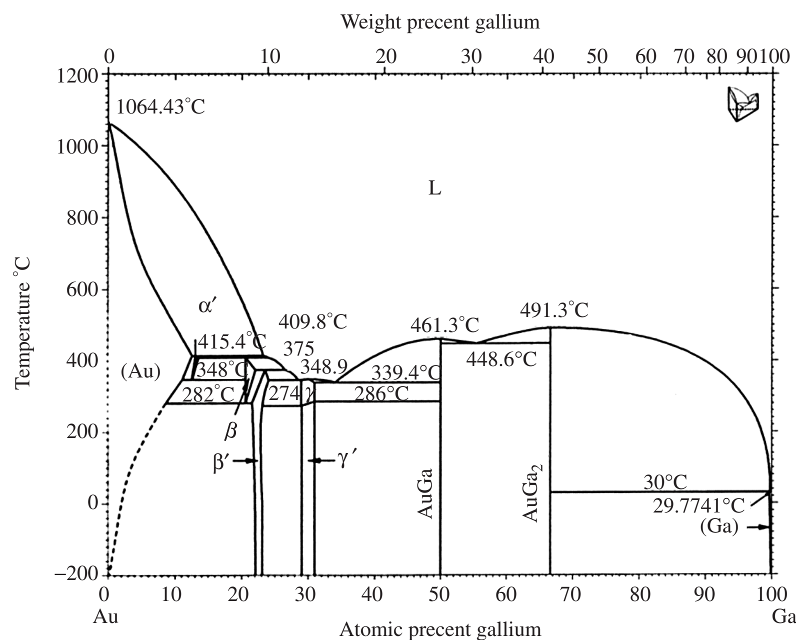


Figure 6. Au-Ga phase diagram. Reprinted with permission from [17], "Binary Alloy Phase Diagrams" (Thaddeus B. Massalski, Editor-in-Chief) (Hiroaki Okamoto, P. R. Subramanian, and Linda Kacprzak, Eds.). ASM International, Materials Park, Ohio, 1990. © 1986, American Society for Metals, Metal Park, Ohio.

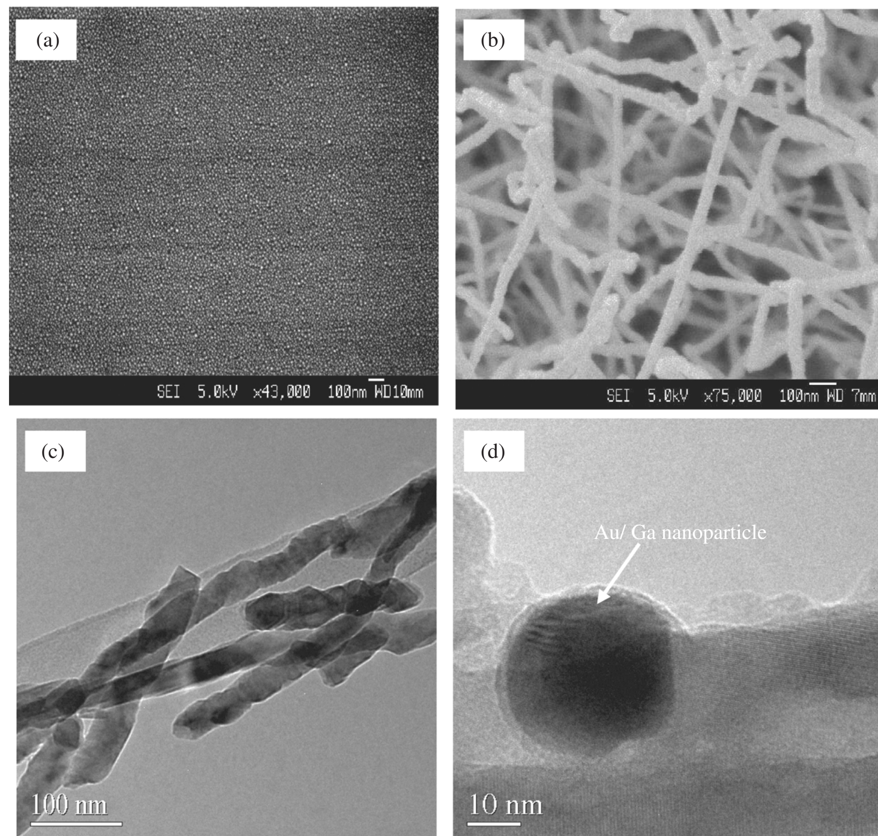


Figure 7. (a) FE-SEM image of Au nano-islands (b) FE-SEM image (c) Low magnification TEM and (c) High resolution TEM image of β-Ga_2O_3 nanowires.

2.1.3. Solution-Liquid-Solid Methods

The synthesis of highly crystalline nanowires of III–V semiconductor by solution-liquid-solid (SLS) at relatively low temperatures was developed by Trentler et al. [18]. The SLS methods follow a similar analogy to the VLS process, in which a low melting point metal (e.g., Sn, In,

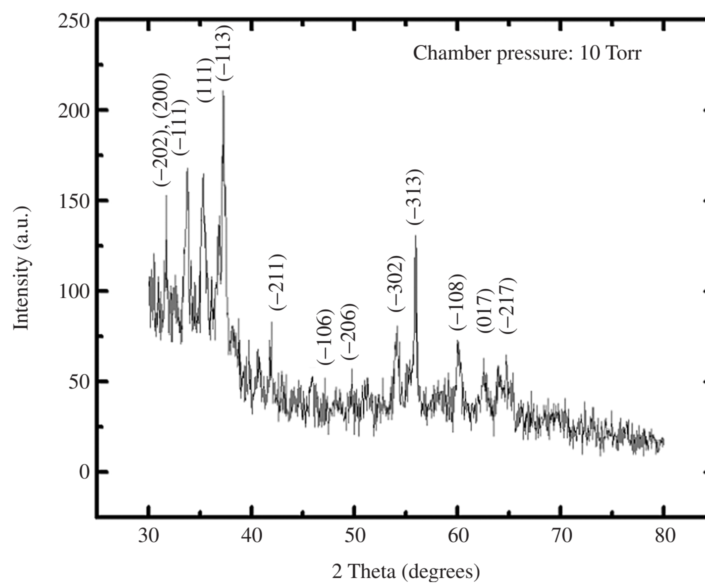


Figure 8. XRD pattern record on the as-deposited Ga_2O_3 nanowires synthesized at 10 Torr chamber pressure. Reprinted with permission from [16], H. M. Lam et al., *App. Phys. A* 79, 2099 (2004). © 2004, Springer.

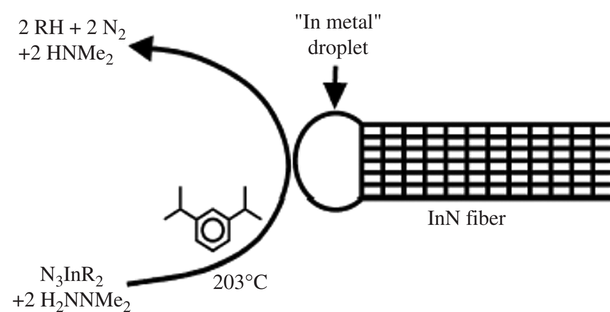


Figure 9. Schematic illustration of the growth of InN nanowire by solution-liquid-solution mechanism. Reprinted with permission from [19], S. D. Dingman et al., *Angew. Chem. Int. Ed.* 39, 1470 (2000). © 2000, Wiley-VCH.

or Bi) is used as the catalyst, and the desired material is generated through the decomposition of the organometallic precursors (Fig. 9). For example, Dingman et al. reported low temperature, catalytic growth of InN fibers from Azido-Indium precursors [19]. Crystalline InN fibers were synthesized at 203 °C, well below the decomposition temperature. They demonstrated that the catalysis effectively lowers crystallization barriers, allowing InN synthesis under solution-phase chemistry. Lu et al. demonstrated the growth of defect-free Si nanowires with uniform diameters of 4–5 nm by using a supercritical fluid as the solvent for SLS process [20]. In their synthesis (Fig. 10), they used monodispersed alkanethiol-capped Au nanocrystals which acts as seeds to direct and control the growth of the Si nanowires

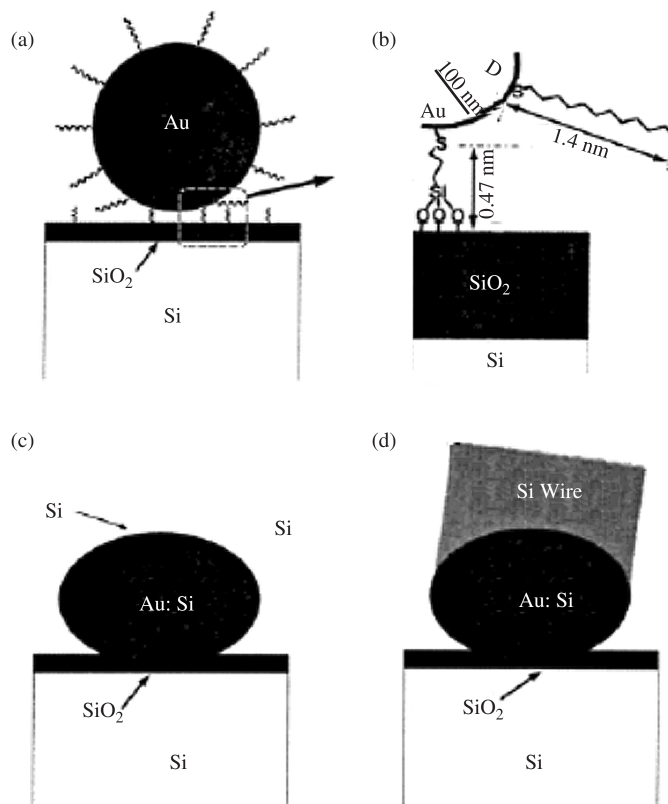


Figure 10. Schematic of Si nanowire synthesis from tethered sterically stabilized Au nanocrystals. (a) Au nanoparticles were adsorbed to an MPTMP-modified Si substrate. (b) Enlarged view of the selected region in (a). (c) DPS degrades to Si atoms that dissolve into the nanocrystals to form Au/Si alloy droplets on the Si substrate. (d) Si nanowires crystallize from the Au nanocrystals seeds upon saturation of the particle. Reprinted with permission from [20], X. Lu, T. Hanrath, K. P. Johnston, and B. A. Korgel, *Nano Lett.* 3, 93 (2003). © 2003, American Chemical Society.

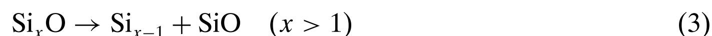
with narrow size distribution. The Au nanocrytals and diphenylsilane co-dispersed in hexane, were heated and pressurized above its critical point. The diphenylsilane decomposed into Si atoms and the Si atoms dissolved into the Au nanocrystals until supersaturation was reached. As a result, Si nanowires were expelled from the Au-Si alloy particle. This growth mechanism shares some similarities with the one proposed by Buhro for the SLS process. More interestingly, the reaction pressure could control the orientation of the Si nanowires.

2.2. Non-Catalytic Methods

2.2.1. Vapor Phase Growth

As early as 1921, Volmer and Estermann observed the formation of Hg nanofibers of 20 nm in diameter when mercury vapor was condensed on a glass surface cooled below the melting point of mercury [21]. In principle, it is possible to synthesize any solid material into 1D nanostructures by controlling the supersaturation at a relatively low percentage. As such, vapor-phase method is probably the most extensively studied approach to the formation of 1D nanostructures such as whiskers, nanowires and nanorods [22]. The driving force for such 1D growth can be explained by the axial screw dislocation and incoming atoms could absorb onto the entire surface of the nanowires and sunsequently migrate to the growing tip. However, no one has been able to observe the proposed screw dislocation in the final product. Now, it is generally accepted that the control of supersaturation is a main consideration in the synthesis of 1D nanostructures as there is strong evidence that the degree of supersaturation determines the prevailing growth morphology. The major advantage of this method is its simplicity and accessibility whereby the vapor species is first generated by evaporation, chemical reduction, and other gaseous reactions. These vapor species are then transported and condensed onto the surface of the solid substrate placed in a zone with temperature lower than that of the source material. One-dimensional nanostructures could be easily obtained with proper control of the saturation factor. Zhang et al. reported the synthesis of Ga_2O_3 and ZnO nanowires by heating commercial powders at elevated temperatures [23]. Figure 11 shows a typical setup for the vapor phase growth of 1D nanostructures. This process involves heating of raw materials with flowing gas at ambient pressure in a horizontal furnace, with no metal catalysts. Nanowires of the raw materials (Fig. 12) are subsequently deposited on the downstream end of the Al_2O_3 tube (lower temperature region).

Although the vapor-phase method looks simple experimentally, their detailed mechanism might involve the formation of intermediates or precursors. As such, decomposition and other secondary reactions also need to be taken into consideration. In a recent study, Shi et al. observed that Si nanowires could be obtained when a mixture of Si and SiO_2 powders was used as the target material for laser ablation [24]. The vapor-phase Si_xO ($x > 1$) generated by laser ablation is suggested to be the key intermediate in this oxide-assisted synthesis. The formation of the silicon nanowires can be explained by the following steps:



$$Si_xO \rightarrow Si_{x-1} + SiO \quad (x > 1) \qquad (3)$$

$$2SiO \rightarrow Si + SiO_2 \qquad (4)$$

Their results suggested that the decomposition reactions first led to the precipitation of the Si nanoparticles encapsulated in the silicon oxide shells. Some of these particles might

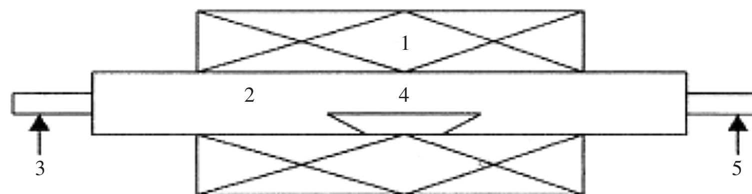


Figure 11. Synthesis system scheme for vapor phase growth of ZnO nanowires (1) furnace, (2) Al_2O_3 tube, (3) gas inlet, (4) Al_2O_3 boat containing raw materials, (5) gas outlet. Reprinted with permission from [23], Y. Zhang et al., *Chem. Mater.* 14, 3564, (2002). © 2002, American Chemical Society.

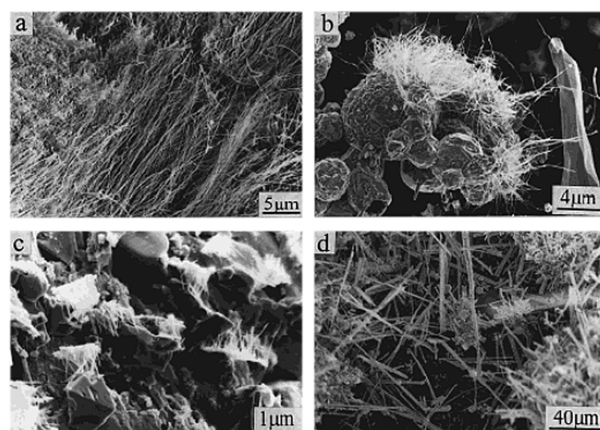


Figure 12. Scanning electron microscopy (SEM) images: (a) Si_3N_4 nanowires, (b) ZnO nanowires, (c) Ga_2O_3 nanowires, and (d) ZnO nanowires synthesized at higher temperature. Reprinted with permission from [23], Y. Zhang et al., *Chem. Mater.* 14, 3564, (2002). © 2002, American Chemical Society.

piled up on the surface of the silicon oxide matrix and served as seeds for the growth of the nanowires in the next step. The major advantage of the oxide-assisted growth is the elimination of the metal catalyst which may cause contamination and altering of the properties of the semiconductor nanowires.

2.2.2. Metal-Organic Chemical Vapor Deposition (MOCVD)

Although this technique has been widely used for epitaxial film growth, it has also been employed for the preparation of 1D nanowires recently. The advantages of MOCVD include large area growth, low deposition temperature, simple and accurate doping, thickness control, high quality and purity deposited products. MOCVD uses MO (metal organic) compound as source of the material, the decomposition of volatile precursors at a suitable temperature in contact with the substrate result in the deposition of the desired product while gaseous side products are easily eliminated. The reaction is carried out inside special reactors (thermal, plasma, laser, or photo activated). Many researchers have employed this technique for the growth of various semiconductor nanowires, such as ZnO [25, 26] Ga_2O_3 [27], GaAs [28] and SiC [29] and etc. Figure 13 shows schematic diagram of the MOCVD setup for the growth of ZnO nanowires [25]. Park et al. demonstrated the epitaxial growth of vertically aligned ZnO nanorods on Al_2O_3 substrates at low temperature of 400 °C [26]. For ZnO nanorods, diethyzinc (DEZn) and oxygen were employed as the reactants and argon was used as a carrier gas. In this process, no metal catalyst was used. The nanorods obtained are of high crystallinity and excellent optical quality.

2.2.3. Template-Confined Growth

In the template-confined growth method, the template serves as scaffold within which a different material is generated *in situ* and shaped into a nanostructure with its morphology complementary to that of the template. When the template is involved physically, post synthesis treatment, such as chemical etching or calcination is necessary to selectively remove the template. On the other hand, in a chemical process, the template is consumed as the reaction proceeds, and it is highly likely to obtain the nanostructures as pure products. It is generally accepted that template-confined growth is a simple, high throughput and cost-effective technique for the synthesis of 1D nanostructures. However, during this procedure, it is difficult to fill the internal nano-channel completely as the removal of solvent may cause structural defects, or hollow or discontinuous growth of nanowires or nanorods. Furthermore, polycrystalline nanostructures are often obtained, with relatively limited quantity. Here, we only briefly discuss four templating methods, with a focus on their feasibility and capability. One-dimensional nanostructures can be generated by employing relief structures on the surface of a solid substrate which acts as templates for directing growth of the nanowires and nanorods.

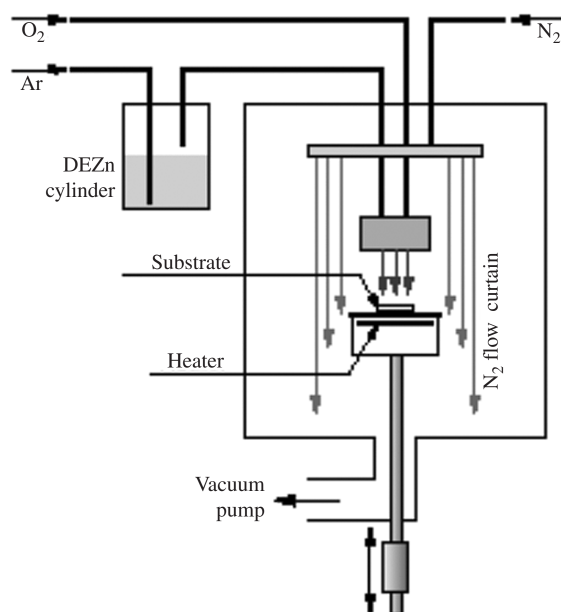


Figure 13. Schematic illustration of the MOCVD reactor used to grow ZnO nanowires. Reprinted with permission from [25], W. Lee et al., *Nanotechnology* 15, 254 (2004). © 2004, Institute of Physics.

These relief structures (V-grooves or step edges) can be patterned efficiently by lithography and etching methods. Techniques for applying the semiconductor at normal incidence [Fig. 15(a)] are based on vapor phase methods such as molecular beam epitaxy (MBE) or solution-phase electrochemical plating. Using this simple method, continuous thin nanowires could be prepared as parallel arrays on the surfaces of the patterned solid substrates, which could be subsequently transferred onto other substrate surfaces in free-standing form. As demonstrated by Muller et al. large parallel arrays of Ge nanowires were fabricated against V-grooves etched in the surfaces of Si substrates [31]. Hulteen et al. [32] pioneered the synthesis of 1D nanostructures by employing channels in porous membranes as templates [Fig. 15(b)]. Two types of porous membranes are commonly used: alumina films containing anodically etched pores and polymer films containing tracked etched channels. Materials can be loaded into the pores using methods based on vapor-phase sputtering, liquid phase injection, solution-phase chemical or electrodeposition. Cleaved-edge overgrowth as shown in Fig. 15(c) has also been used to generate templates (cross-sections of multilayer films) by molecular beam epitaxy (MBE) to grow simple patterns of quantum structures from metals and semiconductors. In this technique, a superlattice consisting of alternating layers such as AlGaAs and GaAs is fabricated by MBE and then cleaved *in situ* through the thickness of the multilayer structure to produce a clean surface. Next, MBE or electrochemical deposition is used to grow epitaxial layers on the selected regions of the exposed surface. This method has demonstrated the formation of intersecting quantum wells with atomic control over the thickness in two directions [33]. Quantum-wire lasers have also been fabricated with this technique [34]. Penner et al. have shown the growth of nanowires by templating against the steps present on a highly oriented, pyroltic graphite using electrodeposition [Fig. 15(d)] [35]. The nanowires were found to preferentially nucleate and grow along the step edges present on the graphite surfaces into 2D parallel array that could be transferred onto other substrate surfaces.

3. CHARACTERIZATION OF SEMICONDUCTOR NANOWIRES

Unique optical, electrical, chemical and thermal properties of 1D semiconductor nanowires make them the key structural blocks for a new generation of nanoscale devices. In many cases, 1D nanowires exhibit superior properties as compared to bulk materials hence it is of-interest to study this new class of intriguing system for the understanding of

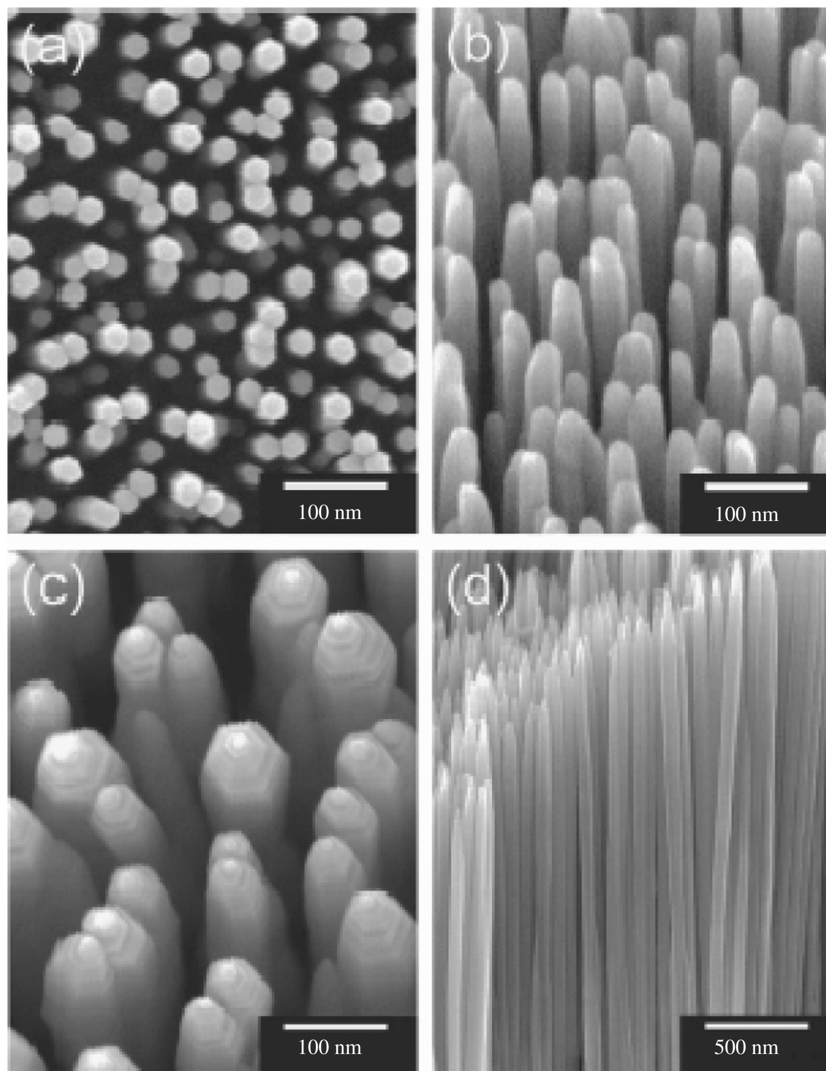


Figure 14. FE–SEM (a) plan-view and (b) tilted images of ZnO nanorods with a mean diameter of 25 nm and (c) tilted and (d) cross-sectional images of ZnO nanorods with a mean diameter of 70 nm. In Fig. 1(c), hexagon-shaped pyramids with flat terraces and steps are shown at the ends of nanorods [26].

the structure-property relationship and related applications of these 1D semiconductor nanowires. This section gives a brief account of the typical properties associated with the semiconductor nanowires.

3.1. Transport Properties

Semiconductor nanowires have been intensively explored as building blocks to fabricate nanoscale electronic devices through a "bottom-up" approach. The prototype devices that have been demonstrated include field-effect transistors, *p–n* junctions, bipolar junction transistors, complementary inverters and resonant tunneling diodes (RTDs) [36]. It is believed that the "bottom-up" or self-assembly approach to nanoelectronics has the potential to go beyond that limits of the traditional "top-down" semiconductor device manufacturing techniques. Hence, the electron transport properties of the nanoscale components become an important issue to study as the critical dimensions of individual devices shrink to the sub-100 nm region. Duan et al. [36] reported selective doping of indium phosphide nanowires that can control the electronic properties of the nanowires. Conductance modulations as large as 4–5 orders of magnitude had been observed. These doped nanowires function as nanoscale field-effect transistors, and can be assembled into crossed-wire *p–n* junctions that

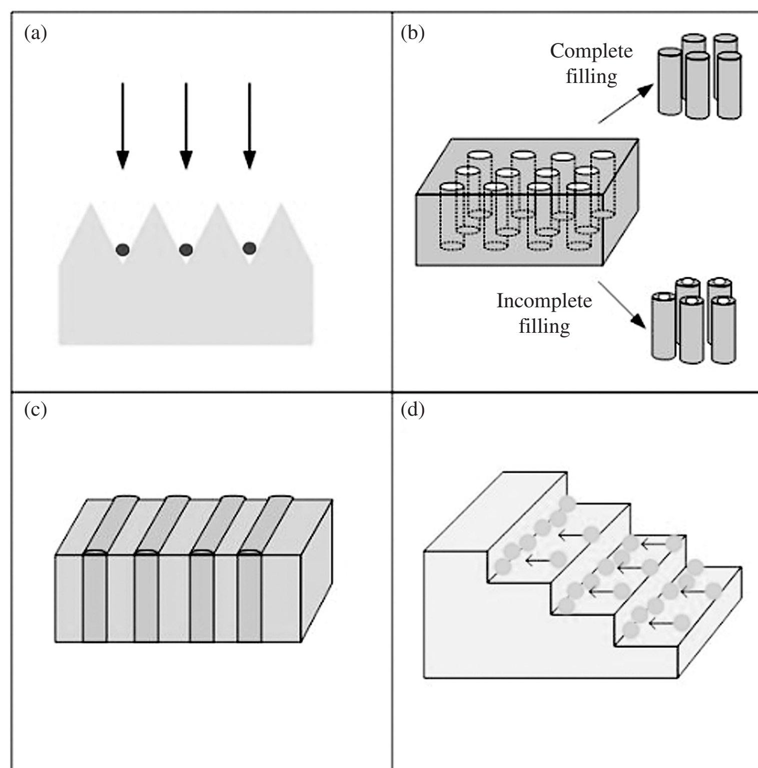


Figure 15. Approaches to 1D nanostructures. (a) Reconstruction at the bottom of V-grooves. (b) Porous membranes can be filled with various materials, creating 1D materials in the channels of the host. (c) Cleaved-edge overgrowth on the cross-section of a multilayer film. (d) Selective deposition of materials on step edges yields nanowires. Reprinted with permission from [30], Y. Xia et al., *Adv. Mater.* 15, 353 (2003). © 2003, Wiley-VCH.

exhibit rectifying behavior as shown in Fig. 16. Recent electrical measurements on a set of nanoscale electronic devices also indicate that GaN and Si nanowires function with good semiconducting properties [37]. The Lieber group at Harvard University furthered demonstrated several GaN nano-field effect transistor, which would be of interest for their high-power/high-temperature electrical applications. On the other hand, transport measurements performed by Chung et al. suggested that Si nanowires became insulating with a thickness of $\sim$15 nm [38].

3.2. Phonon-Transport Properties

As the dimension of 1D nanostructure is reduced to the range of phonon mean free paths (MFPs), the thermal conductivity will be reduced due to scattering at the boundaries. It was found theoretically that the phonon dispersion relation of a silicon nanowire might be modified when its diameter is smaller than 20 nm. Molecular dynamics simulations also showed that the thermal conductivities of Si nanowires could be two orders of magnitude smaller than that of bulk silicon in the temperature range from 200 K to 500 K [39]. Recently, Dames et al. calculated the phonon thermal conductivity of Si/Ge superlattice nanowires by an incoherent particle model [40]. Figure 17 shows the isoconductivity lines as a function of diameters and lengths. Their calculations show that additional sidewall scattering in a superlattice nanowire can reduce the thermal conductivity by a factor of 2 or more. The reduced thermal conductivity finds useful applications in thermoelectric cooling and power generation. So far, good thermoelectrical systems include nanowires made of Bi, BiSb alloy and Bi_2Te_3 [41].

3.3. Optical Properties

Quantum size-confinement plays an important role in determining the energy levels of 1D nanostructures when its diameter is below the critical Bohr radius. Lu et al. found that

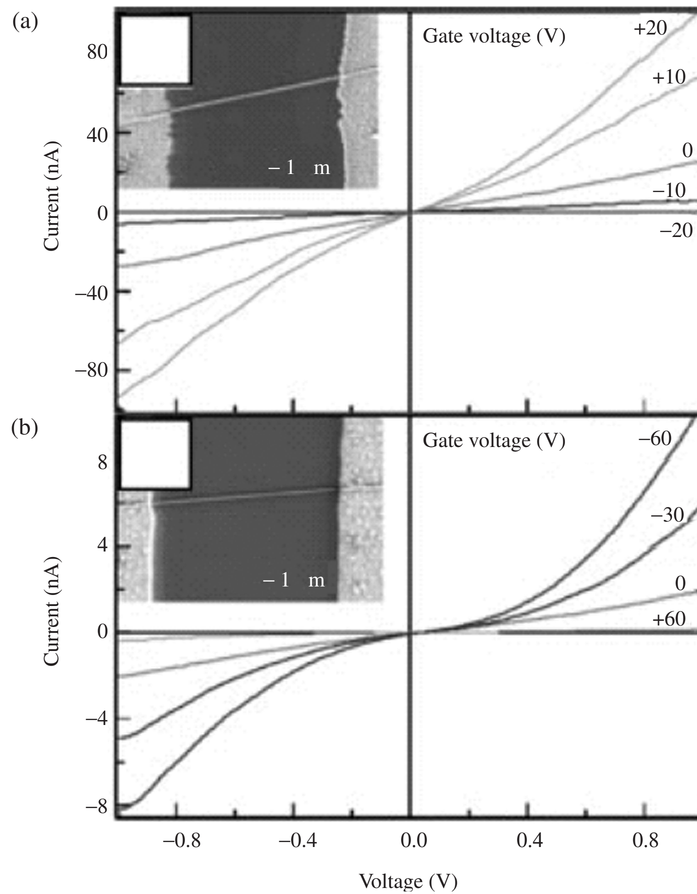


Figure 16. Room-temperature I–V behavior for a Te-doped (a) and Zn-doped (b) InP nanowires at various gate potentials. The inset shows the nanowires sitting across two electrodes. The diameter of the nanowire was 47 and 45 nm, respectively. Reprinted with permission from [36a], X. Duan et al., *Nature* 409, 66 (2001). © 2001, Nature Publishing Group.

the absorption edge of Si nanowires display significant blue shift as compared with the indirect bandgap (∼1.1 eV) of bulk silicon [20]. They observed sharp, discrete features in the absorption spectra and relatively strong band-edge photoluminescence (PL). These different optical features mainly resulted from quantum-confinement effects and also the variation in growth direction for these Si nanowires [42]. In contrast to quantum dots, light emitted from nanowires is highly polarized along the longitudinal axes. Wang et al. [43] showed a

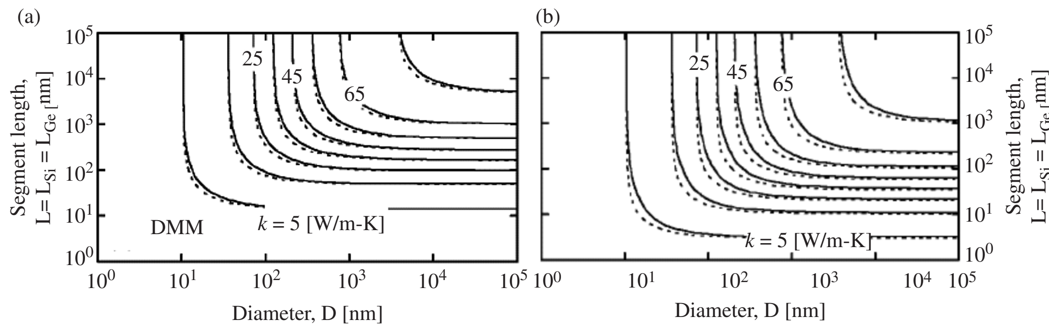


Figure 17. Contours of constant thermal conductivity for a Si/Ge superlattice nanowire as a function of wire diameter D and segment length $L = L_{Si} = L_{Ge}$ at 300 K. (a) Diffuse mismatch. (b) Maximum transmission. The solid lines are the full calculation while the dashed lines are the approximate form of Sec. II G. The conductivity plateau approaches the bulk series average of 78.1 W/m K. Reprinted with permission from [40], C. Dames and G. Chen, *J. Appl. Physics* 95, 682 2004). © 2004, American Institute of Physics.

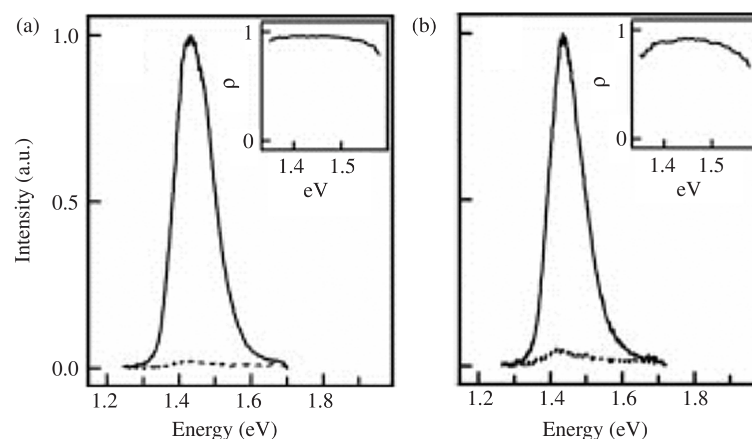


Figure 18. (a) Excitation and (b) emission spectra recorded from an individual InP nanowires of 15 nm diameter. The polarization of the exciting laser was aligned parallel (solid line) and perpendicular (dashed line) to the long axis of the nanowire, respectively. The inset plots the polarization ratio as a function of energy. Reprinted with permission from [43], J. F. Wang et al., *Science* 293, 1455 (2001). © 2001, American Association for the Advancement of Science.

prominent anisotropy in the PL intensities in the direction parallel and perpendicular to the long axes of an individual, isolated indium phosphide (InP) nanowires (Fig. 18). The magnitude of the polarization anisotropy could be quantitatively due to the large dielectric constant contrast between the nanowires and the surrounding environment, as opposed to quantum mechanical effects such as mixing of valence bands.

Lam et al. investigated the photoluminescence of VLS-grown [16] β-Ga_2O_3 nanowires using 325 nm He-Cd laser. Figure 19 shows an emission at 465 nm (blue-green), which indicates a blue shift of 10 nm compared with the PL feature peak 475 nm of bulk β-Ga_2O_3 powder. The blue shifts of β-Ga_2O_3 nanowires can be ascribed to quantum confinement effect. The mechanism of the blue emission of the β-Ga_2O_3 originates from the recombination of an electron on the donor by oxygen vacancies and a hole on the acceptor by gallium vacancies. An electron in a donor band is captured by a hole on an acceptor to form a trapped exciton, which recombines radiatively and emits a blue photon. Oxygen vacancies have been recognized as responsible for the donor band in the Ga_2O_3, while the acceptors would be formed by the gallium vacancies or gallium-oxygen vacancy pairs [16]. Strong

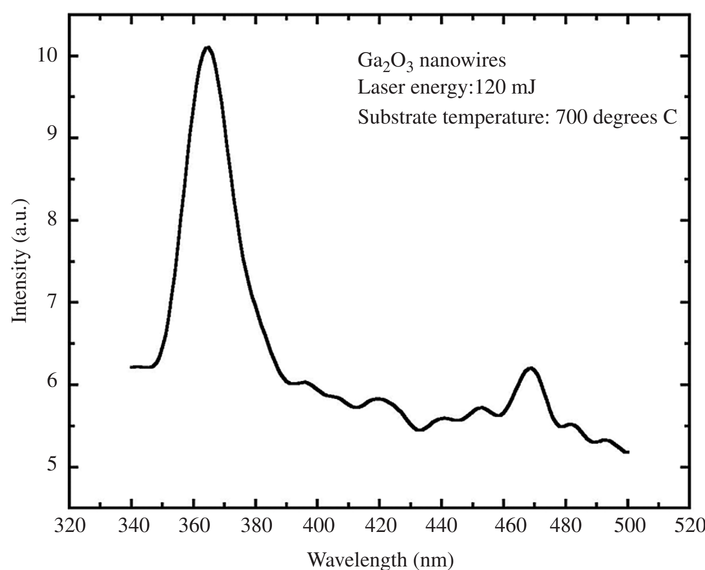


Figure 19. Room temperature PL spectra of β-Ga_2O_3 nanowires under 266 nm excitation.

emission peak at 365 nm (photon energy of ~3.5 eV) indicates strong UV luminescence. This is attributed to intrinsic transition due to recombination of self-trapped excitons. The blue and UV luminescence of β-Ga_2O_3 nanowires may have potential applications in 1D optoelectronic nanodevices.

4. DEVICE APPLICATION OF SEMICONDUCTOR NANOWIRES

4.1. Electronic Devices

a. p–n Junction The most fundamental building block for semiconductor electronic devices is the *p–n* junction that has rectification effect. Mainly two types of *p–n* junction formed by semiconductor nanowire have been demonstrated. The first is cross-bar structure by crossing individually synthesized *p*-doped nanowires and *n*-doped nanowires to form the *p–n* junction at the contact area [44], the second is the internal *p–n* junction formed by dopant modulation during nanowires synthesis [45].

Cui et al. firstly reported controlled doping of silicon nanowires and their transport properties [46]. SiH_4 was used as reactant for Si nanowires synthesis in laser-assisted catalytic growth (LCG) method, B_2H_6 flow and Au-P target together with additional red phosphorous at the reactant gas inlet were used for boron doping and phosphorous doping respectively. The Si nanowires were subsequently placed on back-gated oxidized Si substrate, thermally evaporated Al (50 nm) and Au (150 nm) were thermally evaporated and patterned as contacts. By measuring gate dependent current verse voltage characteristics at the two ends of Si nanowires, one can tell the dopant type in the nanowires and estimate carrier mobility as well. In addition, temperature-dependent studies of heavily B-doped Si nanowires showed no evidence for Coulomb blockade down to 4.2 K, indicating good uniformity in diameter and doping concentration of the Si nanowires to prevent formation of Coulomb islands, in contrast with lithographically patterned Si nanowires. Later Cui et al. also demonstrated rectifying diode structure with crossed *p*- and *n*-type nanowires [44]. A typical configuration is shown in Fig. 20, then *p–n* junction was assembled from 20-nm-diameter *p*- and *n*-type Si nanowires. Current rectification was shown by measurement between contacts 1 and 2 (or 3 and 4). The authors also successfully assembled three-terminal devices with same cross bar scheme, which will be addressed in later part of this session. It is noteworthy that such cross bar scheme is very sensitive to the surface properties of individual nanowires, such as native oxide and dangling bonds at surface, which may significantly affect the carrier transport across the junction [47, 48].

GaN nanowires with internal *p–n* junction were synthesized by turning on an Mg source halfway during VLS process [45]. Mg atoms acted as *p*-type dopant while without Mg dopant the nanowires is *n*-type due to nitrogen vacancies. Current rectifying effect was clearly observed and its temperature dependence was discussed.

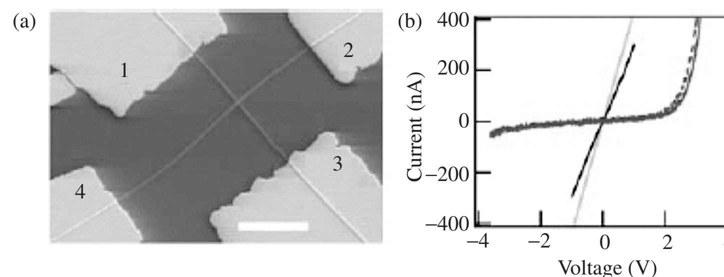


Figure 20. Crossed Si nanowire (SiNW) junctions. (a) Typical FESEM image of a crossed SiNW junction with Al/Au contacts. The scale bar is 2 mm. The diameters of the NWs used in these studies ranged from 20 to 50 nm. (b) The red curves correspond to fourterminal *I–V* through the *p–n* junction; the current values are multiplied by 10. The black and green curves correspond to the *I–V* behavior of individual *p*- and *n*-type SiNWs, respectively. The solid line corresponds to voltage drop measured between leads 3 and 4, and the dashed line to voltage between 3 and 2. Reprinted with permission from [44], Y. Cui and C. M. Lieber, *Science* 291, 851 (2001). © 2001, American Association for the Advancement of Science.

Several methods were used to rule out the possibility of rectifying effect from Schottky metal contact rather than *p–n* junction. The simplest one is to tell from the linear current-voltage characteristics from individual *p*- or *n*-type nanowires. In [49], local nanowire potential was characterized by electrostatice force microscopy (EFM), EFM measurements showed that the entire voltage dropped at the *p–n* junction under reverse bias, while there was no potential drop at the contact under either forward or reverse bias. It is obvious that great progress has been made along the direction of using nanowire as building blocks for various device applications, however, substantial work is still required to ultimately achieve the goal of "bottom-up" manufacturing in the future.

b. Transistor Cui et al. [44] firstly reported transistors made from crossed silicon nanowires. By assembling heavily *n*-doped (emitter) and lightly *n*-doped (collector) across a *p*-type Si nanowires base, a bipolar transistor showed common base current gain of 0.94 and common emitter current gain of 16 respectively. Also switching behavior was clearly shown in a complementary inverter structure made by connecting backgated MOS tansistors assembled with lightly doped *n*-type and *p*-type Si nanowires. Huang et al. investigate the effects of surface oxide on properties of the crossed nanowires [47]. They found that the turn-on voltage of junctions formed by *p*-type silicon and *n*-type GaN nanowires can be changed from about 1 V to around 5 V by increasing the surface oxide layer thickness reproducibly, either by thermal oxidation of the Si nanowires or by passing a high current through the junction in the air. Such high turn-on voltage *p–n* junctions were used as nanoscale FETs and successfully assembled into functional logic gates.

The ease of synthesizing high quality semiconductor nanowire has brought unprecedented flexibility for fabrication of nanoscale devices. Composition and doping modulation can be done along axial as well as radial growth direction, thus the large surface area is utilized for realization of more functions. Lauhon et al. investigated core-shell nanowire homoepitaxy and heteroepitaxy and demonstrated high-performance coaxially gated field-effect transistors [50]. After axial growth of Si nanowires with well-established catalyzed VLS method, radial growth was 'turned-on' by the introduction of diborane, which can lower the decomposition temperature of silane and acts as a *p*-type dopant as well. Post-growth annealing turned the silicon shell layer from amorphous into crystalline. The crystalline *i*-Si/*p*-Si nanowire exhibited low resistivity of (0.5–5) $\times 10^{-3}$ Ω cm and hole mobility of 25 cm^2 V^{-1} s^{-1}, which is comparable with that of single-crystal silicon at similar high doping levels. Using the same method, *i*-Ge/*p*-Si and *p*-Si/i-Ge nanowire structure was also synthesized. The amorphous Si or Ge shell can be completely crystallized by *in situ* thermal annealing at 600 °C. TEM images and elemental mapping both showed that there was abrupt Si-Ge interface (<1 nm). Preliminary electrical transport studies of these structures showed evidence for hole injection from the *p*-Si core to 4-Ge shell. Lastly, coaxial FETs was fabricated with core-multishell structure: *p*-Si/*i*-Ge/SiO_x/*p*-Ge (Fig. 21), where the active channel was the *i*-Ge shell. The device showed good performance with transconductance value up to 1,500 nA V^{-1} at a 1-V source-drain bias, which is comparable to carbon-nanotube FETs.

4.2. Quantum Devices

Analogous to the development from *p–n* junction to quantum well and superlattice by planar semiconductor technology, researchers have explored more quantum confinement effects by composition modulation in the nanowire system. Wu et al. reported synthesis of silicon/silicon-germanium nanowire superlattices using laser ablation growth [51]. Spatially resolved composition analysis showed clearly periodically composition modulation with interface variation on the length scale comparable to the diameter. Similar observation was also made by Lauhon et al. on the GaP/GaAs structure [50].

Bjork et al. studied InAs/InP superlattices grown by nanocluster catalyzed chemical beam epitaxy [52–54] and achieved dislocation-free interfaces with sharpness of 1–3 lattice spacing in 40 nm diameter nanowires as shown in Fig. 22.

Based on such high quality heterostructure they successfully realized double-barrier resonant tunneling device and single electron transistor. In Fig. 23(a) a double barrier device structure is seen in TEM image with 5 nm InP barrier on either side of the 15-nm-thick InAs

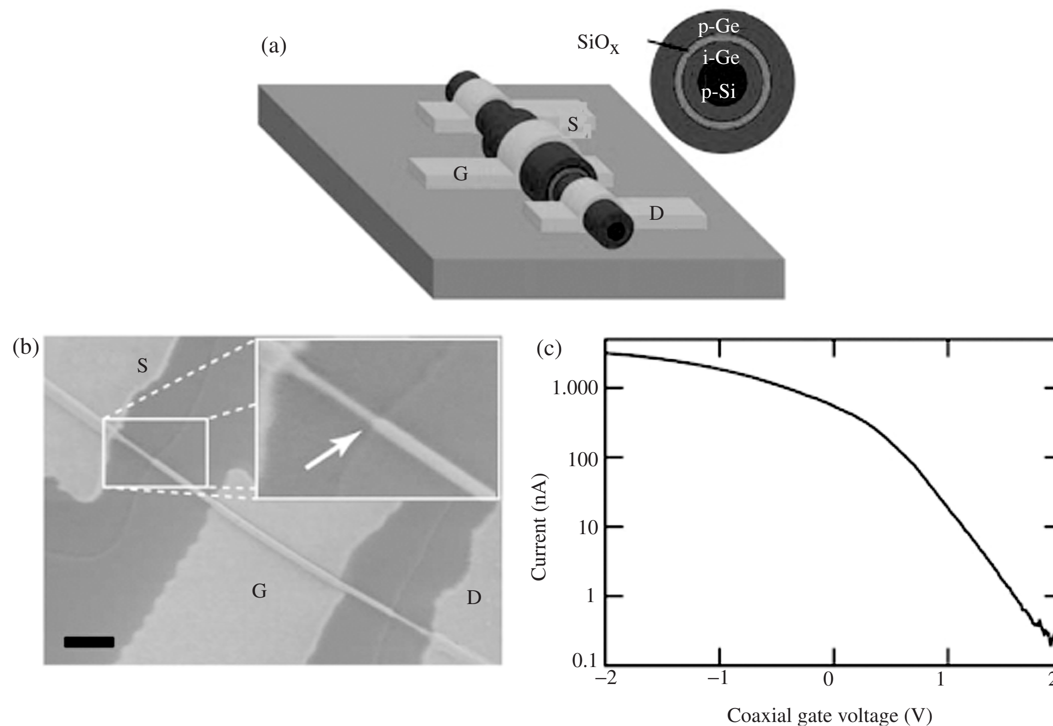


Figure 21. Coaxially-gated nanowire transistors. (a) Device schematic showing transistor structure. The inset shows the cross-section of the as-grown nanowire, starting with a *p*-doped Si core (blue, 10 nm) with subsequent layers of i-Ge (red, 10 nm), SiO_x (green, 4 nm), and *p*-Ge (5 nm). The source (S) and drain (D) electrodes are contacted to the inner *i*-Ge core, while the gate electrode (G) is in contact with the outer *p*-Ge shell and electrically isolated from the core by the SiOx layer. (b) Scanning electron micrograph (SEM) of a coaxial transistor. Source and drain electrodes were deposited after etching the Ge (30% H2O2, 20 s) and SiOx layers (buffered HF, 10 s) to expose the core layers. The etching of these outer layers is shown clearly in the inset and is indicated by the arrow. The gate lectrodes were defined in a second step without any etching before contact deposition. Scale bar is 500 nm. (c) Gate response of the coaxial transistor at $V_{SD} = 1$ V, showing a maximum transconductance of 1,500 nAV^{-1}. Charge transfer from the *p*-Si core to the *i*-Ge shell produces a highly conductive and gateable channel. Reprinted with permission from [50], L. J. Lauhon et al., *Nature* 420, 57–61 (2002). © 2002, Nature Publishing Group.

quantum dot. The expected energy band diagram is shown. It is indicated that the nanowire is *n*-type (because of carbon incorporation during growth even though without intentional doping). The length of the dot determines the longitudinal confinement Due to the tensile strain in the barriers the conduction band offset will be somewhat lower than that for thick barriers, which is 0.6 eV with complete strain relaxation. As the bias is increased the states in the dot will move toward lower energy and, as soon as the lowest dot state is aligned with the Fermi level, which is assumed to lie between the two lowest states in the emitter, the current starts to increase. When the dot-state falls below the energy level of the first emitter state the current drops to zero, resulting in the characteristic negative differential resistance. In Fig. 23(b) the I–V trace for increasing bias voltage (gray) coincides with that for decreasing bias voltage (black), indicating that the device characteristics are highly reproducible and with a high symmetry of the device structure.

Single-electron transistors were also fabricated using InAs/InP heterostructure nanowires. As shown in Fig. 23(c). at temperature of 4.2 K, clear coulomb blockade of the current on the InAs island between the InP barriers was observed and can be periodically lifted as a function of backgate voltage. For the 55 nm diameter nanowires with a 100 nm long InAs island, the charging energy is 4 meV and the conduction oscillations are visible up to roughly 12 K, for which the thermal energy is 1 meV. Compared to the above-mentioned InAs/InP RTD with an InAs island length of 15 nm, the energy level splitting is very small, thus no negative differential resistance was observed.

Park et al. reported catalyst-free fabrication of ZnO/ZnMgO nanorod heterostructures by MOCVD [55]. The multiple quantum well (MQW) nanorods prepared in their study consist

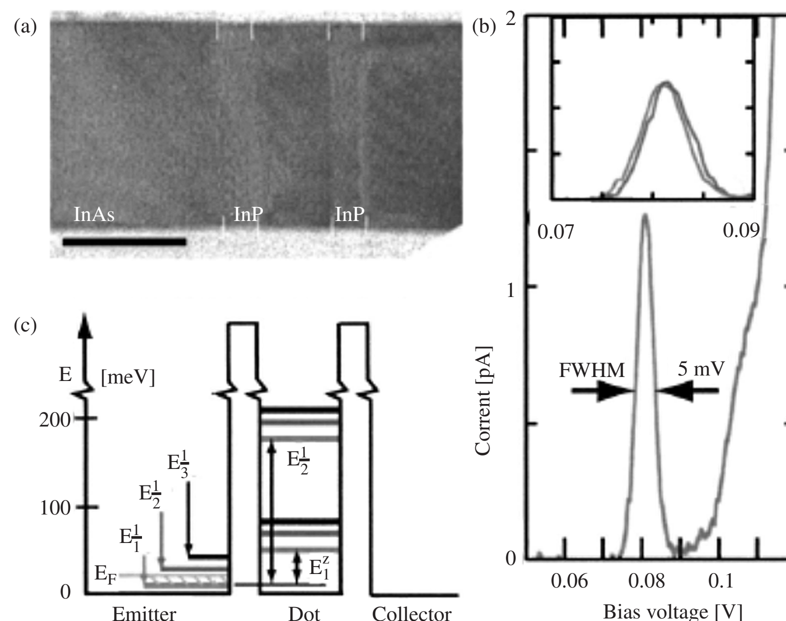


Figure 22. Double-barrier resonant tunneling data for devices fabricated inside a nanowire. (a) TEM image of the top end of a nanowire with the double barrier clearly visible, in this case with a barrier thickness of about 5 nm (scale bar depicts 30 nm). (b) The principle of the energy band diagram for the device investigated with the characteristic electronic states in the emitter region indicated (left). (c) Current–voltage data for the same device as shown in (a) and (b) recorded at 4.2 K, revealing a sharp peak in the characteristics, with a voltage width of about 5 mV. The robustness of the device characteristics is shown in the inset, which provides a magnified view of the resonance peak for increasing voltage (gray) and for decreasing voltage (black), hence, confirming negligible hysteresis effects. Reprinted with permission from [53], C. Thelander et al., *Appl. Phys. Lett.* 83, 2052 (2002). © 2002, American Institute of Physics.

of 10 periods of Zn0.8Mg0.2O/ZnO on ZnO nanorods; vertically grown and well-aligned, as depicted in Fig. 24. They found that the atomically abrupt interfaces present in the MQW heterostructures achieved well-defined potential profiles with nanosized well structure in individual nanorods that are tunable through the quantum confinement effects. Figure 25 presents the well-width dependent blue shift resulting from quantum confinement. The blue shift decreases with increasing well width and is almost negligible at well width of 110 Å. The ability to grow quantum well heterostructures nanorods is expected to greatly increase the versatility and power of these building blocks for applications in nanoscale photonics and electronics.

4.3. Light Emitting Devices

Various optoelectronics devices including LEDs, lasers, photodetectors and photonic switches have been made from different kinds of nanowires. Duan et al. studied electroluminescence (EL) from crossed *p*-type and *n*-type InP nanowires [56]. They verified that the EL was originated from the forward biased *p–n* junction and observed blue shift of maximum intensity. Increasing blueshift with decreasing diameters was attributed to quantum confinement of excitons.

Several groups studied photoresponse of semiconductor nanowires such as InP, ZnO, In_2O_3 [57, 58] and showed that nanowires can be easily made into photodetectors. Wang et al. also found the unique highly polarized photoluminescence and detection properties of InP wires [57]. It is expected that nanowires can opens up exciting opportunities for the creation of a wide range of detectors and high-resolution detector arrays for different spectral regimes.

Nanowires are good candidate for laser devices because quantum effects can result a substantial density of states at the band edges and enhance radiative recombination due to carrier confinement thus the can achieve lower lasing threshold, also the optical confinement and electrical confinement can be easily implemented. Huang et al. have observed

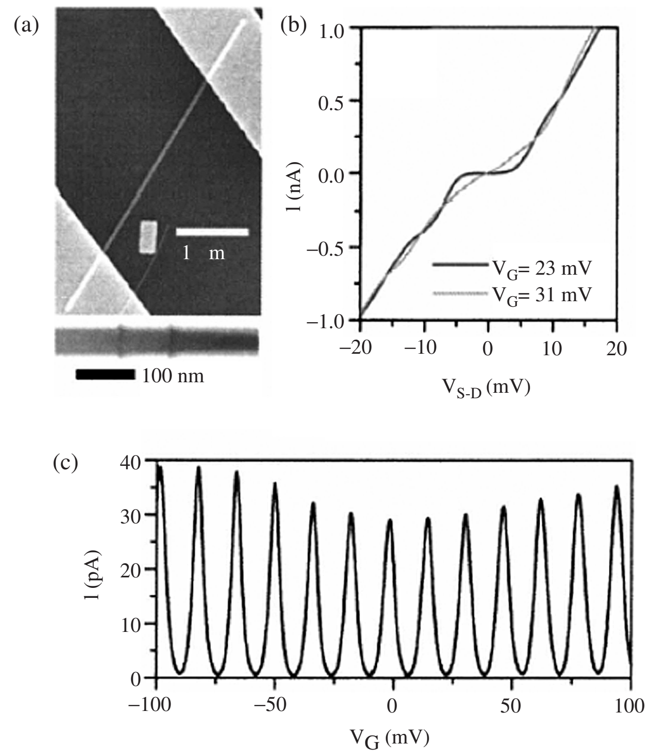


Figure 23. (a) Scanning electron micrograph of an electrically contacted InAs nanowire with an InP double-barrier structure. The lower inset shows how a selective InAs etch can be used to reveal the InP double barrier (transmission electron micrograph). (b) *I–V* curves for the 55 nm diameter device in (a) recorded for two different gate voltages at $T = 4.2$ K, corresponding to a blocked (black) and a conducting state (gray). (c) Current through the device plotted as a function of the universal back-gate voltage for $V_{SD} = 0.5$ mV. Reprinted with permission from [54], M. T. Björk et al., *Appl. Phys. Lett.* 81, 4458 (2002). © 2002, American Institute of Physics.

room-temperature UV-lasing from arrays of ZnO nanorods grown on sapphire substrates using the VLS method [59]. A typical setup for lasing experiments is depicted in Fig. 26(a), one end of the nanowires was terminated in the epitaxial interface between sapphire and ZnO, and the other end in the flat (0001) plane of hexagonal ZnO [Fig. 26(b)]. They achieved

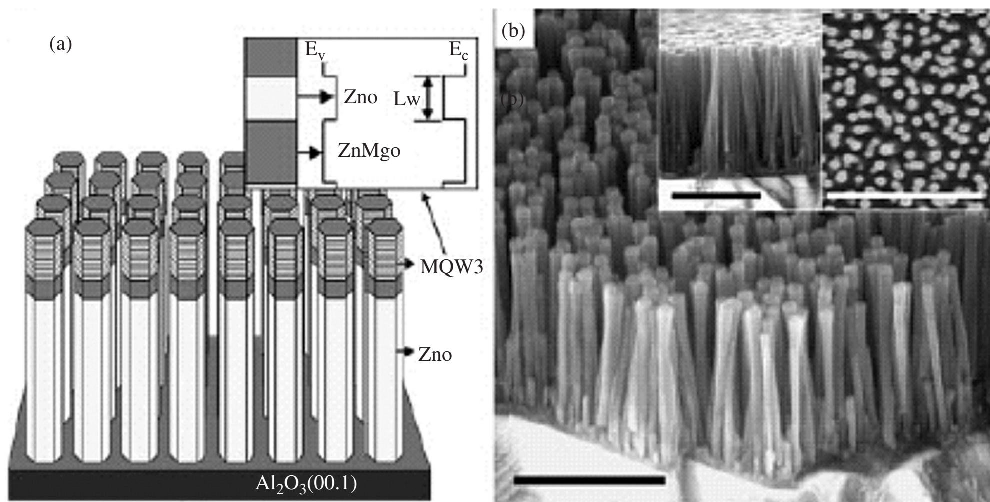


Figure 24. (a) Schematic of multiple quantum well (MQW) nanorods consisting of 10 periods of $Zn_{0.8}Mg_{0.2}O/ZnO$ on the tips of ZnO nanorods. An electronic band diagram for the MQW is inset. (b) FE-SEM images of the MQW nanorods. Scale bar: 0.5 μm. Reprinted with permission from [55], W. I. Park et al., *Adv. Mater.* 15, 526 (2003). © 2003, Wiley-VCH.

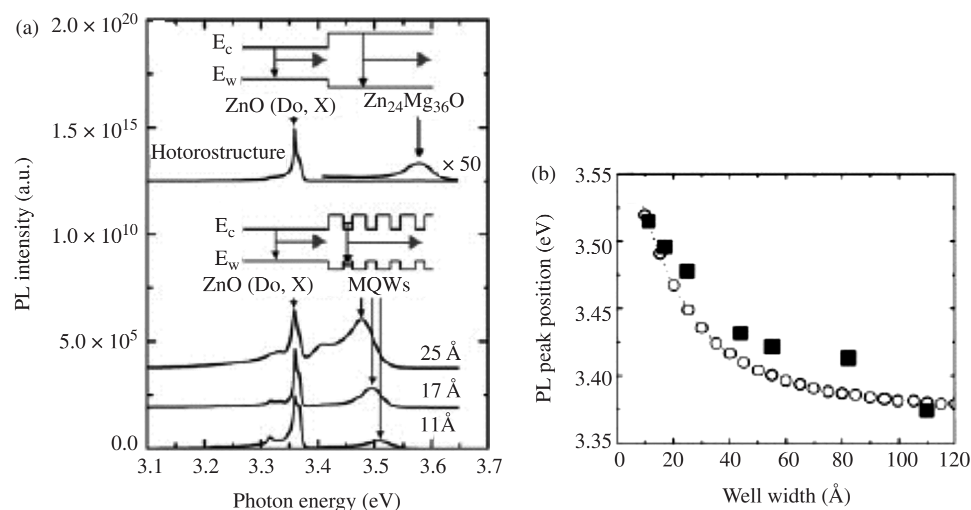


Figure 25. (a) 10 K PL spectra of $Zn_{0.8}Mg_{0.2}O$/ZnO heterostructure nanorods and $Zn_{0.8}Mg_{0.2}O$/ZnO MQW nanorods with band diagrams shown inset. (b) Well-width dependent PL peak in $Zn_{0.8}Mg_{0.2}O$/ZnO MQW nanorods (squares) and theoretically calculated values (circles) in 10 periods of 1D square potential wells. Reprinted with permission from [55], W. I. Park et al., *Adv. Mater.* 15, 526 (2003). © 2003, Wiley-VCH.

good position, orientation, diameter and density control of ZnO nanowires growth and demonstrated their optical-pumped lasing properties. Using a fourth harmonic of Nd:YAG laser (266 nm, 3ns pulse width) at room temperature as optical pump source at an incidence angle of 10° to the symmetric axis of the nanowire, sharp peak (with line width

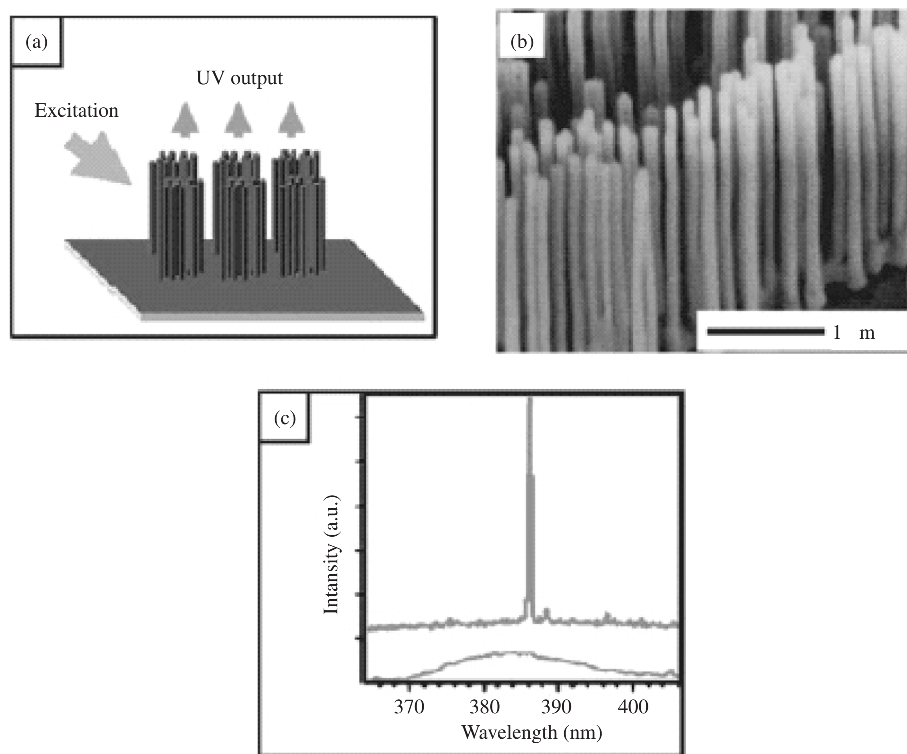


Figure 26. (a) Schematic illustration of the excitation and detection configuration used for the lasing study (b) SEM image of a 2C array of ZnO nanowires grown as uniaxial crystals on the surface of a sapphire substrate. (c) The power-dependent emission spectra recorded from a 2D array of ZnO nanowires, with the excitation energy being below (bottom trace) and above (top trace) the threshold. Reprinted with permission from [59], W. I. Park et al., *Appl. Phys. Lett.* 80, 4232 (2002). © 2002, American Institute of Physics.

less than 0.3 nm) lasing action was observed in the direction normal to the end surface plane of nanowire. The threshold is about 40 kW cm^{-2}, which is significantly less than that (~300 kW cm^{-2}) in disordered particles or thin films.

The lasing effect in nanowires was also confirmed by optically characterizing individual ZnO nanowires using near-field scanning microscopy [60]. The observation of lasing action in ZnO nanowires without the fabrication of mirrors shows that single-crystalline, well-facetted nanowires can function as effective resonance cavities. Figure 27 depicts an example where the nanowires were excited with short pulses (<1 ps) of 4.35 eV photons (285 nm) in order to observe PL and lasing. The emission from an individual nanowire was collected using a chemically etched fiber optic probe. Both topographic and optical information could be collected simultaneously during the forward and reverse scans.

In a more recent study, Johnson et al. also observed lasing in GaN nanowires [61]. The chemical flexibility and one-dimensionality of these nanowires make them ideal candidates for fabricating nanoscale laser light sources which will find applications in nanophotonics and microanalysis. Yu et al. also investigated random laser action with coherent feedback, in ZnO nanorod arrays embedded in ZnO epilayers depicted in Fig. 28 [62]. Figure 29 shows the light-light curves and emission spectra of the sample. Threshold pump intensities of TE and TM polarizations are found to be about 800 kW/cm^2 and 1.6 MW/cm^2, respectively. The lasing intensity of TM polarization is weaker than that of TE polarization, which is due to the orientation of the ZnO nanorods. In this study, they demonstrated that random laser action can also be supported in ZnO nanorod arrays as they verified that the dependence of threshold pump intensity on the excitation area agrees well with the random laser theory.

Significantly, electrical-driven CdS nanowire-based laser was successfully implemented by Duan et al. [63]. The CdS nanowires used are single-crystal wurtzite structure with a [001] growth axis. The diameter is 80–20 nm. Noticeably high yield of flat ends perpendicular to the [001] growth direction were produced at a high yield (>50%) by sonication which ensure the nanowires to function as Fabry-Perot cavities.

High excitation power photoluminescence measurements showed that the end-emission intensity increased superlinearly with excitation power. In addition, periodic variations in the intensity indicated Fabry-Perot cavity was formed, the estimated moderate cavity quality

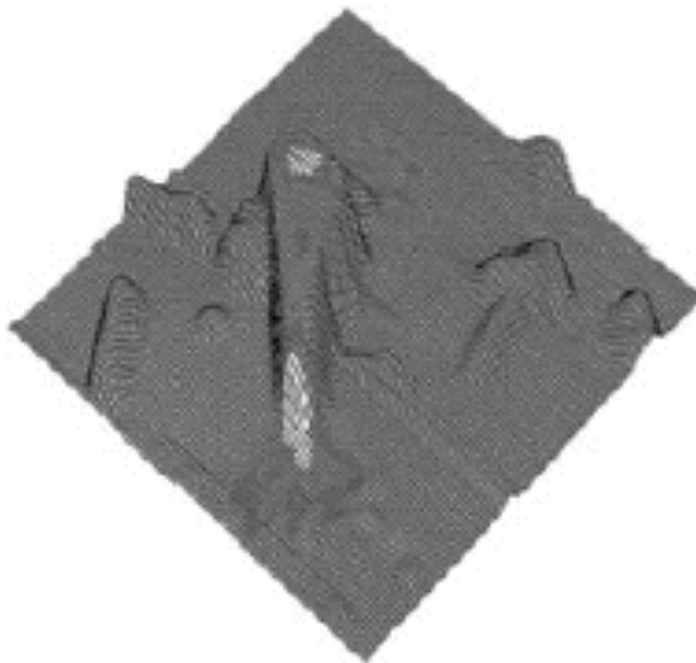


Figure 27. Near field optical image of an individual lasing ZnO nanowires. Note that the lasing emission is only seen at the two ends of these nanowires. Reprinted with permission from [60], J. C. Johnson et al., *J. Phys. Chem.* 105, 11387 (2001). © 2001, American Chemical Society.

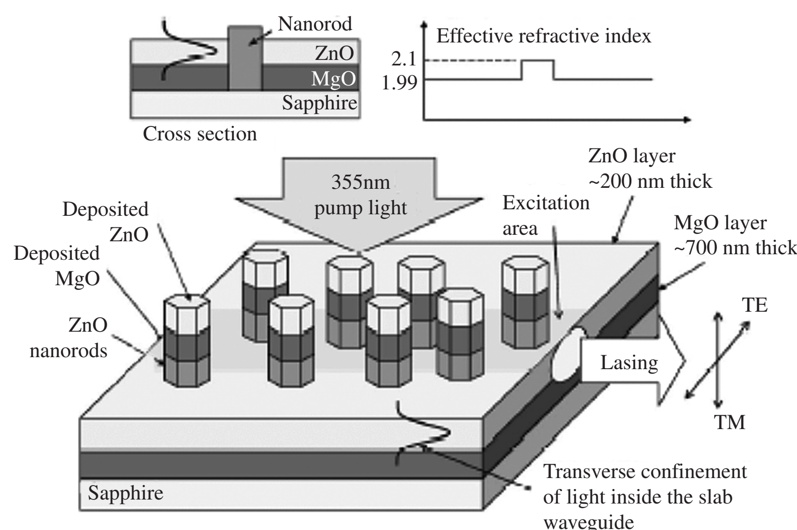


Figure 28. Schematic diagram of the ZnO nanorods embedded in the ZnO epilayers. Bottom half of the diagram shows the arrangement of optical excitation of the sample. Top half of the diagram shows the cross section of the sample and the corresponding effective refractive index of the slab waveguide and ZnO nanorods. Reprinted with permission from [62], S. F. Yu et al., *Appl. Phys. Lett.* 84, 3241 (2004). © 2004, American Institute of Physics.

factor of about 600 at room temperature. Subsequently optical pumped lasing was observed with the lowest threshold value of around 2 kW cm^{-2} at low temperature. Finally electrically driven lasing was achieved by a hybrid structure shown in Fig. 30, in which heavily p-doped silicon was used for hole injection to circumvent the problem in producing high mobility p-type CdS. Electroluminescence measurements showed that at current level higher than 200 μA the spectrum quickly collapsed into a very sharp peak(s) with linewidth less than 0.3 nm, which is clearly a characteristic of lasing.

4.4. Photoconductivity and Optical Switching Devices

Recent work from several groups demonstrated that it is possible to fabricate highly sensitive electrical switches by controlling the photoconductance of individual semiconductor nanowires. For instance, Kind et al. observed that the conductance of ZnO nanowires was extremely sensitive to ultraviolet light irradiation [64]. The light-induced insulator-to-conductor transition enabled them to reversibly switch a nanowire between OFF and ON

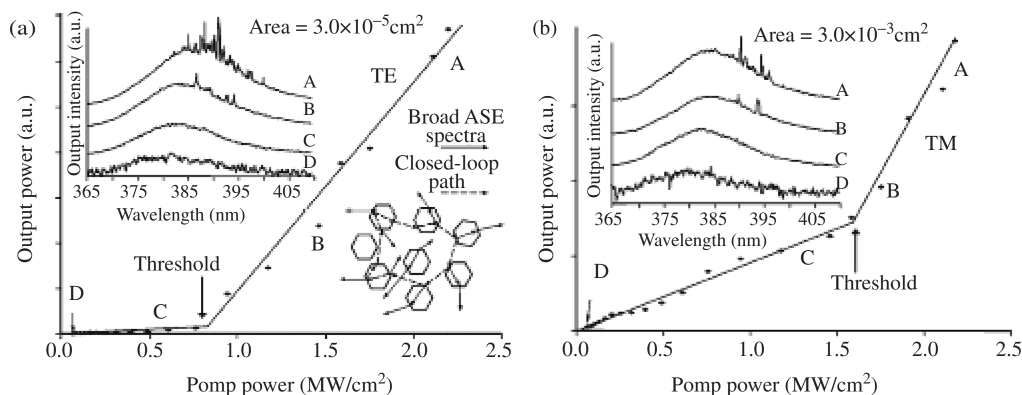


Figure 29. Light–light curves and emission spectra of (a) TE polarization and (b) TM polarization form the ZnO nanorods embedded in ZnO epilayers. The insets on the top-left-hand side corner is the emission spectra at various pump intensities and that on the bottom-right-hand side corner is a schematic diagram showing the formation of closed-loop path for light through recurrent scattering (dashed arrow) and single-broad ASE spectra (solid arrow) in the sample. Reprinted with permission from [62], S. F. Yu et al., *Appl. Phys. Lett.* 84, 3241 (2004). © 2004, American Institute of Physics.

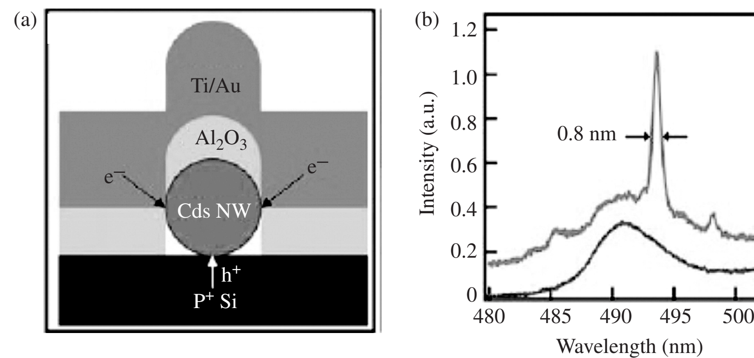


Figure 30. Nanowire electrical injection laser. (a) Schematic showing the cross-section of the device structure. In this structure, electrons and holes can be injected into the CdS nanowire along the whole length from the top metal layer and the bottom *p*-Si layer, respectively. The devices were fabricated by assembling CdS nanowires on heavily doped *p*-Si on insulator substrates, followed by electron beam lithography and electron-beam evaporation of 60–80 nm aluminum oxide, 40 nm Ti and 200 nm Au. One end of the nanowire was left uncovered for emission output from the device. (b) Emission spectra from a CdS nanowire device with injection currents of 200 mA (lower curve) and 280 mA (upper curve) recorded at 8 K. The spectra are offset by 0.10 intensity units for clarity. The single peak observed at high injection has a linewidth of 0.8 nm, comparable to the instrument resolution and that observed in the optical pumping experiments. Reprinted with permission from [63], X. Duan et al., *Nature* 421, 241–245 (2003). © 2003, Nature Publishing Group.

states. In a typical experiment, four-point probe measurements on individual ZnO nanowires indicated that they were essentially insulating in the dark. However, upon exposure to UV light with wavelength below 400 nm, their resisitivity was significantly reduced. In addition to their high sensitivities, they also show excellent wavelength selectivity. Figure 31(a) shows a ZnO nanowire displaying photoresponse under UV light (365 nm) exposure, while there is no photoresponse at all to the green (532 nm) light. Measurements on the spectral response show that the ZnO nanowires indeed have a cut-off wavelength at 385 nm which is well-agreed with the bandgap of ZnO. With this observation, Kind et al. furthered evaluated the photoconductive characteristics of the ZnO nanowires. Figure 31(b) shows the photoresponse of a ZnO nanowire as a function of time while the UV lamp was switch on and off. They observed that the nanowires could be reversibly and very rapidly switched ON and OFF. Their demonstration suggested that these photosensitive nanowires could serve as UV light detectors in applications such as microanalysis and missile plume detection as well as fast switching devices.

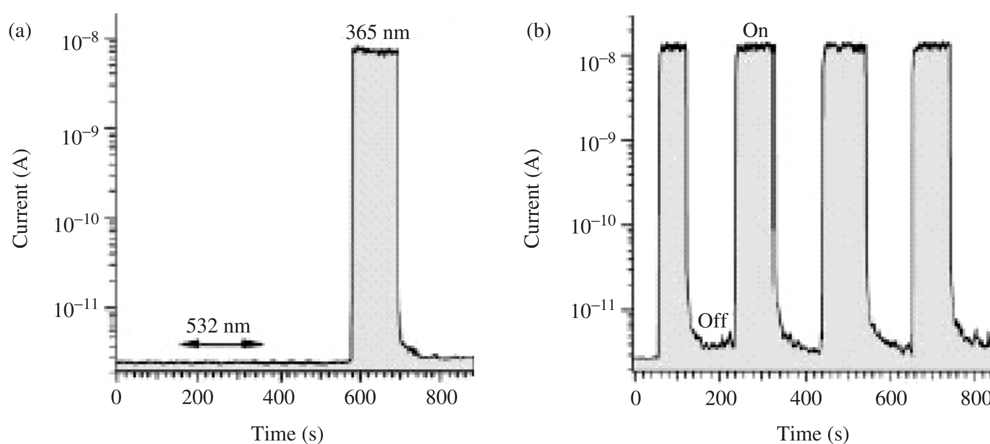


Figure 31. (a) The photoresponse (change in current under a constant bias) of a ZnO nanowires to light exposure at two different wavelengths: 532 nm and 365 nm. (b) Reversible switching of a ZnO nanowire between its low and high conductivity states. Reprinted with permission from [64], H. Kind et al., *Adv. Mater.* 14, 158, (2002). © 2002, Wiley-VCH.

4.5. Sensors

One-dimensional nanostructures have yet another important application related to the sensing of important molecules, either for medical, environmental, biological or security-checking purposes. The extremely high surface-to-volume ratios associated with these nanostructures make their electrical properties very sensitive to species adsorbed on the surfaces. Recently Law et al. fabricated the first room-temperature photochemical NO_2 sensors based on individual single crystalline oxide nanowires and nanoribbons [65]. They demonstrated the concept of SnO_2 nanowires as an example. Tin dioxide is a wide bandgap (3.6 eV) semiconductor. For the *n*-type SnO_2 single crystals, the intrinsic carrier concentration is determined by oxygen vacancies, which are predominantly atomic defects. The electrical conductivity of nanocrystalline SnO_2 depends strongly on surface states produced by molecular adsorption that often lead to space-charge layer changes and band modulation. Nitrogen dioxide acts as an electron-trapping adsorbate on SnO_2 crystal surfaces and can be detected by monitoring the electrical conductance of the material. As NO_2 chemisorbs strongly on SnO_2 surfaces, commercial thin-film SnO_2 sensors have to be operated at 300–500 °C to enhance the surface molecular desorption kinetics and continuously "clean" the sensors. The high temperature operation in this case is not favorable, especially in an explosive environment.

Law et al. [65] found that the strong photoconductive nature of individual single-crystalline SnO_2 nanobelts makes it possible to achieve equally favorable adsorption–desorption behavior at room temperature by UV illumination of the SnO_2 devices, near its bandgap. They studied the optoelectronic response of these nanowires in air and NO_2 environments in order to determine their chemical sensing abilities. Figure 32 shows the conductance response of one nanosensor cycled between pure air and 3 ppm NO_2. The resolution limit achieved by these oxide nanobelts fell between 2–10 ppm. Even with low signal/noise ratio, current steps could be clearly distinguished as the NO_2 source was turned on and off. This behavior was stable for more than 20 cycles without noticeable drift and the response times could be kept shorter than 1 min. These measurements indicated that individual oxide nanobelts are small, fast and sensitive devices for detecting ppm-level NO_2 at room temperature with UV light exposure. Here the advantages of the oxide nanobelts for low-temperature, almost drift-free operations make them good candidates for nano-sized, ultra-sensitive gas sensors in many applications.

4.6. Field Emission Applications

Nanotubes and nanowires with sharp tips are promising candidates for applications related to cathode, field emission of electrons. Zhou et al. have investigated the field emission (FE) characteristics of Si and SiC nanorods using current-voltage measurements [66]. Both nanorods

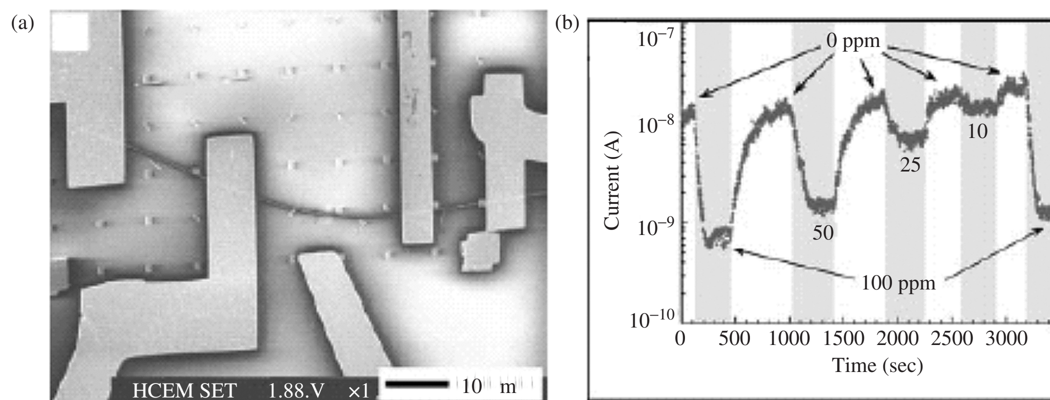


Figure 32. (a) SEM image showing a SnO_2 nanobelt spanning across four electrodes of a transport measurement setup. (b) Cycling a nanosensor near its resolution limit under 365 nm light with a bias of 0.5 V. The concentrations of NO_2 are indicated. The horizontal bars represent averaged signals. The difference in average signals for these 3 cycles was 16%. Reprinted with permission from [30], Y. Xia et al., *Adv. Mater.* 15, 353 (2003). © 2003, Wiley-VCH.

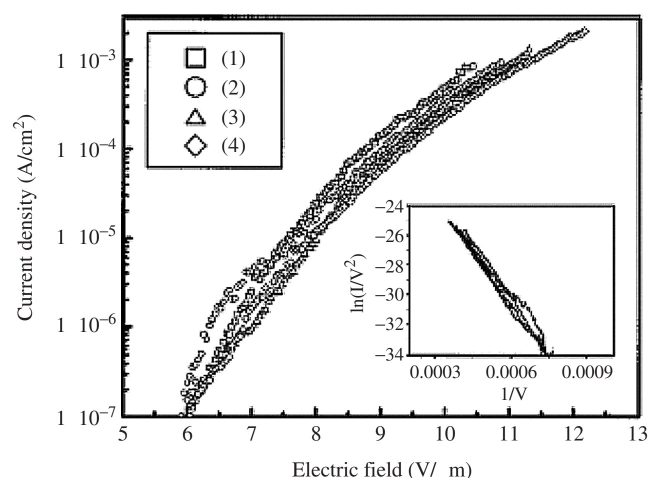


Figure 33. Emission current density from ZnO nanowires grown on silicon substrate at 550 °C. The inset reveals that the field emission follows FN behavior. Reprinted with permission from [67], C. J. Lee et al., *Appl. Phys. Lett.* 81, 3648 (2002). © 2002, American Institute of Physics.

exhibited good and robust field emission. The turn-on field for Si and SiC nanorods was 15 and 20 V/μm, respectively, and the current density of 0.01 mA/cm^2 was comparable with those observed for other field emitters made of CNTs and diamonds. The SiC nanorods exhibited a particularly high electron emission, as well as good stability. Also in a recent publication, Lee et al. also studied the field emission properties of well-aligned ZnO nanorods grown on a low-temperature CVD method [67]. The turn-on voltage for the ZnO nanowires was found

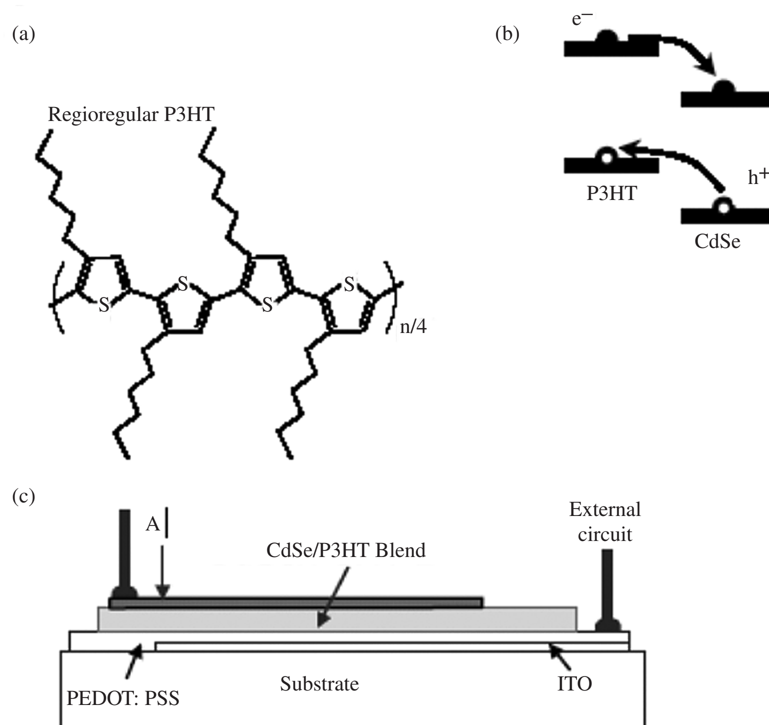


Figure 34. (a) The structure of regioregular P3HT. (b) The schematic energy level diagram for CdSe nanorods and P3HT showing the charge transfer of electrons to CdSe and holes to P3HT. (c) The device structure consists of a film ~200 nm in thickness sandwiched between an aluminum electrode and a transparent conducting electrode, which was deposited on an indium tin oxide glass substrate. The active area of the device is 1.5 mm by 2.0 mm. This film was spin-cast from a solution of 90% wt% CdSe nanorods in P3HT in a pyridinechloroform solvent mixture. Reprinted with permission from [69], W. U. Huynh et al., *Science* 295, 2425 (2002). © 2002, American Association for the Advancement of Science.

to be about 6.0 V/μm at current density of 0.1 μA/cm^2 (Fig. 33). The emission current density from the ZnO nanowires reached 1 mA/cm^2 at a bias field of 11.0 V/μm. Recently, Li et al. [68] achieved excellent field emission properties of ZnO nanowires synthesized by a metal catalyzed VLS process. Their results showed a turn-on field of 0.83 V/μm and corresponding current density of 25 μA/cm^2 [68]. The emitted current density of the ZnO nanowires is 1.52 mA/cm^2 at a bias field of 8.5 V/μm. The large field emission area factor, β arising from the morphology of the nanowire field emitter, is partly responsible for the good emission characteristics. The ZnO nanowires with high emission current density and low turn-on field are expected to find use as active components in fabricating field-emission display devices.

4.7. Photovoltaic Applications

Huynh et al. [69] recently demonstrated the use of semiconductor nanorods to enhance the possibility and efficiency of solar cells, as shown in Fig. 34. They made thin-film photovoltaic devices by blending CdSe nanorods with polythiophenes to obtain nanocomposite materials.

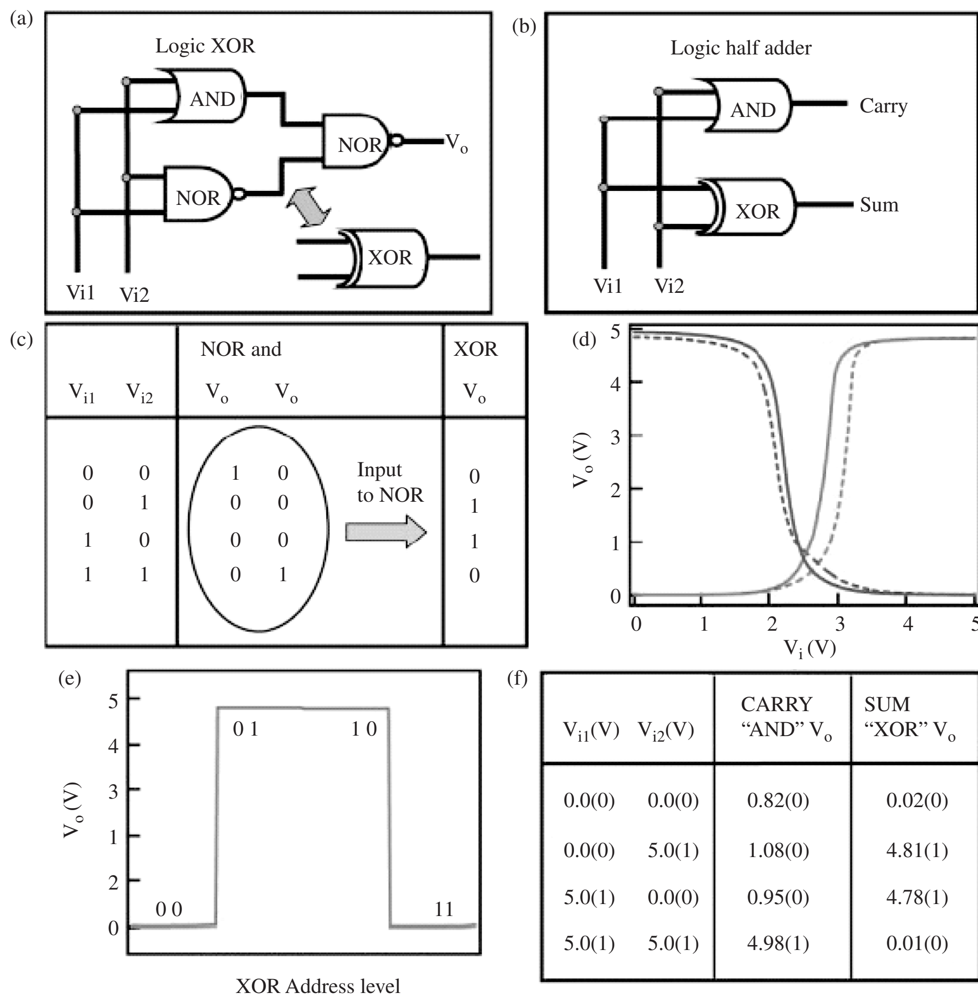


Figure 35. Nanowire computation. (a) Schematic of logic XOR gate constructed with the output from an AND and a NOR as the input to a second NOR gate. (b) Schematic for logic half adder. (c) Truth table for logic XOR gate. (d) XOR output voltage versus input voltages. The solid and dashed red (blue) lines show V_o–V_{i1} and V_o–V_{i2} when the other input is 0 (1). The slope of the V_o–V_i data shows that the gain exceeds 10. The XOR gate was achieved by connecting the output electrodes of an AND and NOR gate to two inputs of another NOR gate. (E) The output voltage versus the four possible logic address level inputs for the XOR gate. (F) Experimental truth table for the logic half adder. The logic half adder was obtained by using the XOR gate as the SUM and an AND gate as the CARRY. Reprinted with permission from [56], Y. Huang et al., *Science* 294, 1313 (2001). © 2001, American Association for the Advancement of Science.

The features and performance of such a device could be tuned by controlling the aspect ratios of the nanorods. They also discovered that nanorods were superior to quantum dots in photovoltaic applications as they could provide a direction path for electrical transport at much lower loadings. Under Air Mass (AM) 1.5 Global solar conditions, a power efficiency of as high as 1.7% has been achieved.

5. ASSEMBLY AND INTEGRATION

To realize the substantial potential of bottom-up manufacturing paradigm with semiconductor nanowires, it is imperative to develop efficient methods to assemble the high quality semiconductor nanowires into well-ordered structures. In addition, the versatility to integrate nanowire from different semiconductor materials has been made possible.

Huang et al. successfully developed microfluidic method to directly assemble the synthesized nanowires into networked as desired [70]. Logic functions were implemented using such network in a controllable manner [47]. By passing suspensions of the nanowires through fluidic channel structures formed between a poly (dimethylsiloxane) (PDMS) mold and a flat substrate, nanowires can be assembled into parallel with control of separation. Higher flow rate resulted in better degree of alignment and longer flow duration led to higher nanowires density with spacing on the order of 100 nm or less. It was also found that the surface chemical functionality will significantly affect the deposition rate and minimum separation. Most importantly, sequential flow steps do not affect the deposited nanowires thus hierarchical assembly of nanowires into multiple crossed array were successfully achieved by changing the flow direction between different layers. Compared with other assembly approaches such as direct manipulation of individual nanowires [71] and control by electric fields [56], the microfluidic method is more efficient, cost-effective and scalable.

Utilizing the well-developed microfluidic method, Huang et al. demonstrated logic OR, AND and NOR gates with *p*-type silicon nanowires and *n*-type GaN nanowires [56]. By combination of multiple AND and NOR gates they were able to implement basic computation in the form of and XOR gate and a half adder, as shown in Fig. 35. Also Zhong et al. reported address decoder based on nanowires crossbar arrays [72] in which selective chemical modification of cross points in the array enhanced the performance of the crossed nanowires field-effect transistor (CNW-FET) thus enabled nanowires inputs to turn on and off specific FET array elements with gain.

Most recently, simulations were carried to access the 16 Kbit nanowires-based electronic nanomemory system [73]. The system consisted of three nanowires devices: crossed nanowires that form the nonvolatile nanowire diodes, the top-gated nanowires field effect transistors (TGNW-FETs) and nanowire interconnects. Empirical behavior of the three devices was modeled using commercially available analog hardware description language (analog HDL), then the empirical device model was incorporated into the Cadence Spectre simulator. Banking strategy was adopted by combining smaller nanomemory array into big one to allow the same level of defect tolerance with less redundancy. Ziegler et al. presented the relation between estimated area per usable bit with respect to nanowires pitch for different memory arrangement and it is shown that when the nanowires pitch is approximately 15 nm the bit density can reach goal of DAPPA's Moletronics Program in 2005 of 1011 bits/cm^2, in contrast with the ITRS projection of commercial DRAM densities of 13×1010 bits/cm^2 by 2006 [73]. The dissociation of nanowires growth and device fabrication have enabled combination of different semiconductor materials to form high performance building blocks with great flexibility.

Another scheme is to integrate wafer level patterned and aligned nanowires growth with subsequent conventional planar semiconductor processes. Wang et al. reported hexagonal-patterned growth of aligned ZnO nanorods [74]. Martensson et al. demonstrated nanowire array defined by nanoimprint lithography [75]. Most noticeably, Nguyen et al. implemented fabrication of In_2O_3 nanowires into vertical field-effect transistor [76].

After synthesis of single crystalline semiconductor indium oxide (In_2O_3) vertically and uniformly on sapphire substrate covered with In_2O_3 thin film, fabrication of vertical field-effect transistor (VFET) was carried out. First silicon diode was deposited with chemical deposition

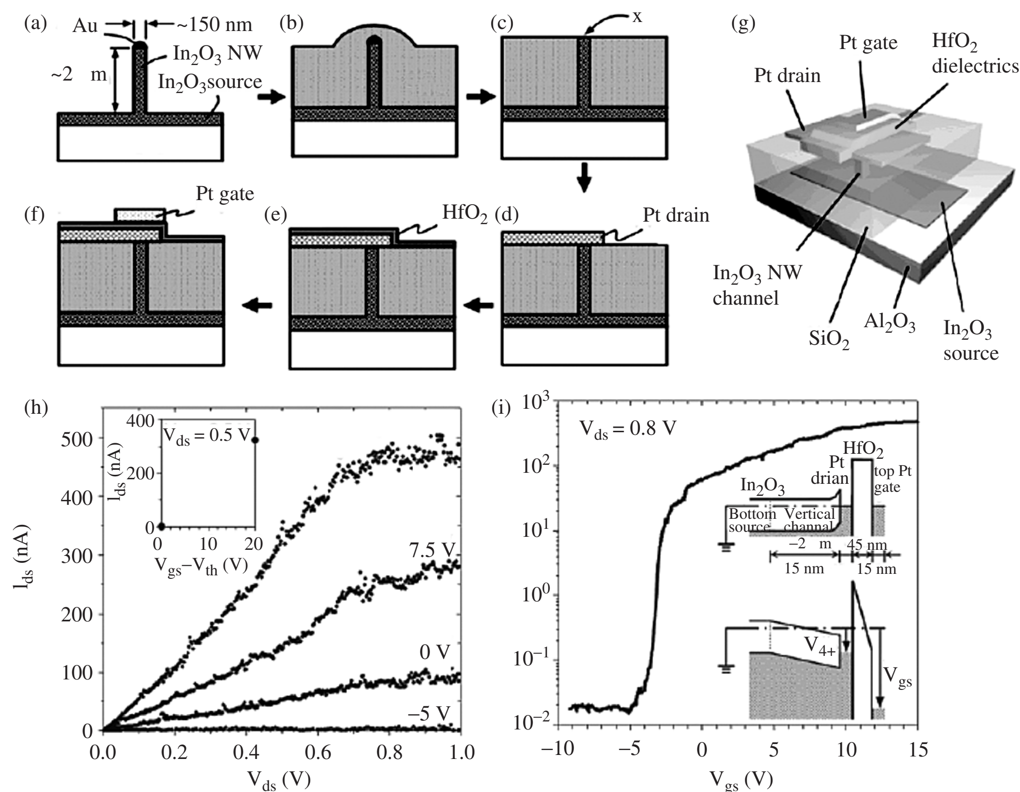


Figure 36. Vertical field-effect transistor (VFET) process flow and I–V characteristics. (a-f) A schematic of a process flow showing the major steps taken to fabricate an In_2O_3 integrated VFET. Cross-sectional views are shown for the various fabrication stages. (a) A vertical In_2O_3 nanowire-integrated *a*-sapphire (Al_2O_3) substrate. The underlying In_2O_3 buffer layer serves as the bottom source while the vertical In_2O_3 nanowire acts as the active electron channel. (b) Conformal chemical vapor deposition of silicon dioxide (SiO_2) to encapsulate the nanowire completely. (c) Chemical mechanical polishing (CMP) to remove the excess SiO_2 and expose the tip of the nanowire (denoted by x). The Au alloyed head is also removed during the CMP process. (d) Formation of a top Pt drain electrode (150 Å thickness). (e) Selective patterning of HfO_2 dielectrics (450 Å thickness), which serves as the gate oxide. (f) Formation of a top Pt gate electrode (150 Å thickness). (g) A 3D schematic illustrating the various components of a completed VFET. (h) I_{ds} vs. V_{ds} characteristics of a VFET with V_{gs} as a parameter. The inset shows a I_{ds} vs V_{gs}–V_{th} plot. (i) Transfer characteristics of a VFET at $V_{ds} = 0.8$ V. The top inset shows a band diagram of the VFET in equilibrium with $V_{gs} = V_{ds} = 0$ V while the bottom inset shows that in operation with $V_{gs} \gg V_{ds} > 0$ V.

process at 700 °C, whereby the In_2O_3 nanowire was conformally surrounded and encapsulated. Then a chemical mechanical polishing step was used to planarize and fully expose the top of the nanowire in addition to removal of Au alloyed head. Subsequently a top platinum (Pt) electrode (150 Å thickness) was lithographically patterned on the exposed end of the nanowire to provide an electrical contact as the drain electrode of the VFET. This was followed by introduction of 450 Å thickness hafnium oxide to form the gate dielectrics. Finally Pt tope gate electrode was made. A 3D schematic illustrating is shown in Fig. 36. With I_{ds} vs. V_{ds} characteristics and transfer characteristics. Gate controlled transistor behavior was clearly demonstrated in such an unconventional field effect structure. Fine-tuning of process and optimization in structure of such nanowire-based VFET has the potential to achieve tera-level ultrahigh density circuits.

6. CONCLUSIONS

Tremendous progress has been achieved in the semiconductor nanowire synthesis which enables successful demonstration of various kind of electronic and optoelectronic devices.

More precise nanowire synthesis besides composition, doping, diameter and length control will enable fine tuning of the material property and device function. Most recently, Wu et al. showed crystalline orientation dependence on diameter of silicon nanowire [79],

Kuykendall et al. accomplished crystallographic alignment of high-density gallium nitride nanowire arrays [80].

With availability of such high quality nanowires, in-depth investigation of quantum confinement effects in such system and their impacts on device performance is imperative. A typical problem is carrier transport investigation in nanowire structures. Nanowire-based field effect transistor is a good candidate for future-generation microelectronics [81]. However, electron transport in these nanowires remains an open question. Cui et al. reported that thermal annealing and chemical passivation of oxide defects could increase transconductace and mobility of silicon nanowire field effect transistor [48] while simulation results from Kotlyar et al. suggested that mobility in narrow silicon nanowires is significantly degraded because of increased electron-phonon wave function overlap [82]. Further investigation on electron-phonon interaction in such system needs to be carried out to settle the debate.

The development in this direction remains to be fast. Just to name a few, recently Han et al. reported a new versatile synthetic approach to produce high-quality, single crystalline transition metal oxide nanowires on nanowire templates with presence of metal-insulator transition [77], Wu et al. demonstrated high quality metal/semiconductor nanowire heterostructures with atomically sharp metal-semiconductor interfaces and fabricated field-effect transistors in which metallic NiSi nanowire region defined source-drain contacts [78]. It is foreseeable that novel devices with wide spectrum of properties such as superconductivity, ferroelectricity and colossal magnetoresistivity etc. will be developed in these nanowire structures.

In summary, nanowire-based electronic and optoelectronic devices hold promise for future and there will be more interesting topics to be explored.

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